TANDY®

Service Manual

26-3930

Tandy® WP-2 Portable Wordprocessor

Catalog Number: 26-3930

SPECIFICATIONS

Microprocessor	NEC 70008A-6(Z80 type)		
Clock Speed	5.5296 MHz		
Memory	256 KByte Standard ROM (BIOS, WORDPROCESSOR, and spell check), 32 KByte Standard RAM (VRAM and Free Area) ROM: Option (IC Card) Expandable up to 256 Kbyte RAM: Option (RAM chip) Expandable 32 Kbyte or 128 Kbyte (RAM Disk) Option (IC Card) Expandable 32 Kbyte, 64 Kbyte, 128 Kbyte (IC Card)		
Keyboard	Full-size 62 keys.		
Display	"Supertwist" LCD, 480 × 64 pixels, 8 × 80 characters		
	AC Adapter		
External Connections	DB-25 Parallel Printer		
	DB-9 Serial Port		
	DIN-8 Cassette Tape		
	IC Card-38 Memory Card		
Battery	AA size battery × 4, Alkaline or Ni-Cd		
AC Adapter	6 VDC 400 mA, UL listed (Cat. No. 26-3804)		
	UNIT	NORMAL	LIMIT
Power Consumption (at 6VDC)	mA	80 – 90	140

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I. SYSTEM OVERVIEW

This manual has been prepared for Tandy technicians working in the field or in repair centers. Users of this manual should be acquainted with the μPD70008A-6 microprocessor and the 82C51 UART.

The Tandy WP-2 has the following applications programs in the standard ROM: TEXT, TELCOM, PHONE(ADDRESS), CALENDAR(SCHEDULE), SPELLCHECK, and FILES.

I-1. External View

1. Keyboard: Can be used like a standard typewriter. However, the Tandy WP-2 does have a few special keys. (See Appendix C of this manual for more details.)

2. LCD Screen: The Tandy WP-2 display is eight lines by 80 characters.

3. Power Switch: Pressing this switch turns the power on and off. To conserve the batteries, the Tandy WP-2 automatically turns the power off if you do not use it for 10 minutes in the default setting.

4. CONTRAST control: This control adjusts the contrast of the LCD display.

5. PROTECT Switch: This switch is used to prevent discharge of the Lithium battery, used for RAM back up. The Tandy WP-2 operates only when the power switch is set to ON. Set this switch to the OFF position when the Tandy WP-2 will not be used for a long period of time. Note that the RAM is not backed up when this switch is set to the OFF position, and all information RAM in will be lost.

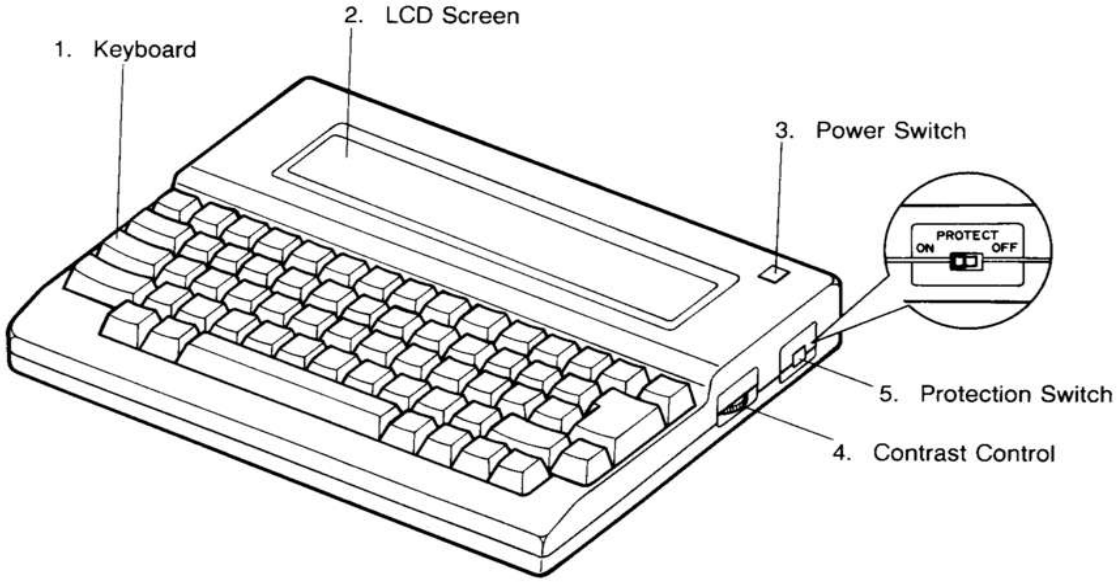


Figure 1-1. Front View

1. Expansion Card (IC Memory) Slot: Insert the IC memory card into this slot. The connector in the slot is connected to the system bus of the CPU.

2. Serial Interface Connector (RS232C): Attach a DB-9 cable (such as Radio Shack Catalog Number 26-265) to this connector when you need to receive or transmit serial information. This connector is also used for the FDD.

3. Printer Interface Connector: For hard-copy printouts of information, attach any Radio Shack parallel printer to this connector, using an optional/extra printer cable.

4. Cassette Interface Connector: To save or load information on a cassette tape, connect the cassette recorder here. An optional/extra cassette recorder cable is required.

5. AC Adapter Jack: Connect the appropriate end of Radio Shack's AC adapter (Catalog Number 26-3804, optional/extra) to this connector. Connect the other end of the AC adapter to a standard AC wall-outlet or approved power strip.

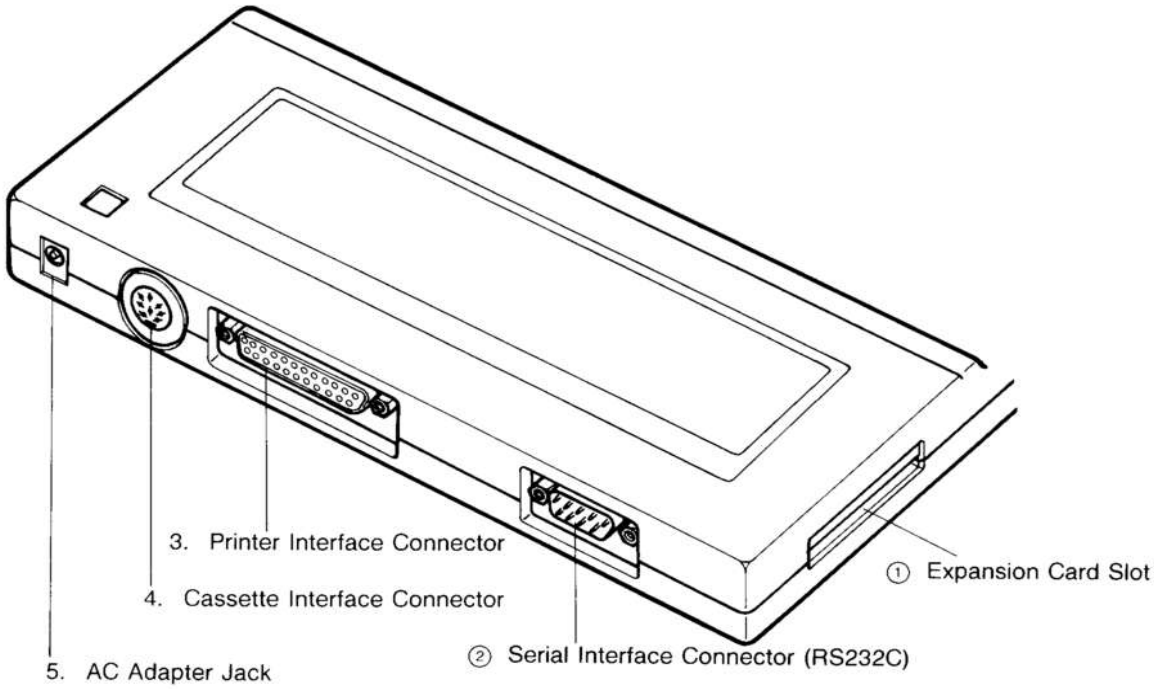


Figure 1-2. Rear View

1. Main Battery Compartment: When an AC adapter is not connected, the Tandy WP-2 gets its power from four AA size batteries installed in this compartment.

2. Back-up Battery Compartment: The Tandy WP-2 gets RAM back-up power from a Lithium battery (CR-2430) installed in this compartment.

3. RESET Button Hole: If the Tandy WP-2 locks up (i.e., the display "freezes" and all keys seem to be inoperative), push this button; the display returns to the Main menu (start-up). All data stored in RAM will be lost when you press RESET.It is not likely that the Tandy WP-2 will lock up when you are using the built-in applications programs. However, it might occur with customized programs.

4. Stands: Pull down to make the WP-2 sit at an angle.

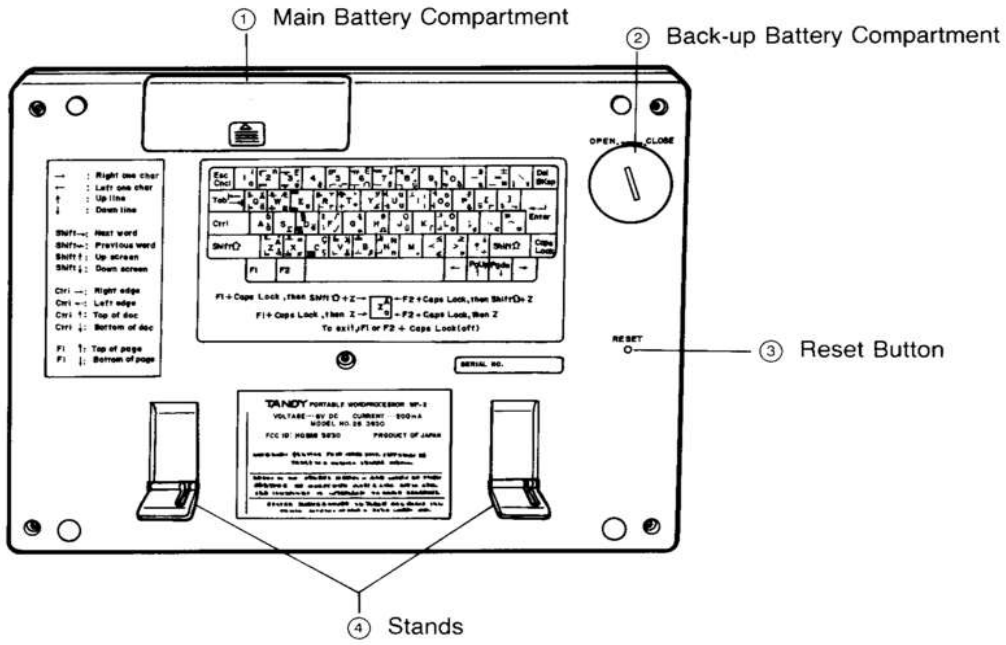


Figure 1-3. Bottom View

I-2. Internal View

Optional RAM Compartment: An optional RAM can be inserted into this compartment to enhance the Tandy WP-2 capabilities.

The Tandy WP-2 consists of four printed circuit boards:

* LCD PCB
* Keyboard PCB
* Main PCB
* Sub PCB

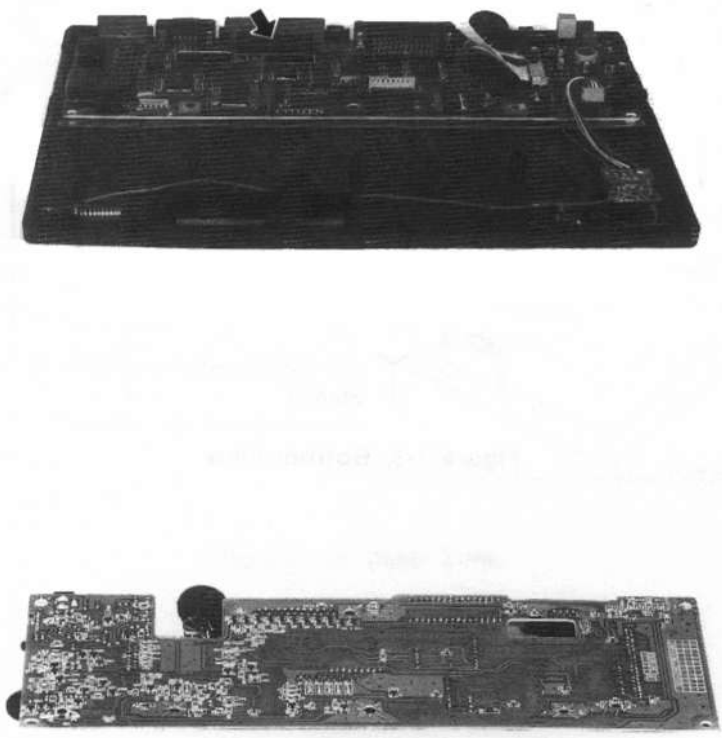


Figure 1-4. Main PCB (Bottom View and Top View)

Figure 1-5. LCD PCB

I-3. Specifications

Main Components

Keyboard	
Life of keyboard	500 million keystrokes
Number of keys	62 keys (8 × 8 key matrix)
All keys	Keys can be pressed down a distance of 3 millimeters.
Power switch	Press the switch down 1 millimeter to turn the WP-2 on or off.
LCD display	
Display panel	480 × 64 full-dot matrix
Dot pitch	0.44 × 0.44 mm
Dot size	0.41 × 0.41 mm
Effective display area	211.16 (W) × 28.12 (D) mm
Operation batteries	
Batteries	Type AA × 4 Alkaline-manganese batteries
Operation time (approximately)	3.5 days (typ.)-4 hours per day 14 days (typ.)-1 hour per day (Note: Without I/O units at normal temperature)
Memory protection battery	
Battery	Lithium battery (270 mAh/3.6V)
Back-up time	More than 3 years 32 KByte RAM 1.5 years (typical) 32 KByte + 32 KByte RAM option 1.5 years (typical) 32 KByte + 128 KByte RAM option
LSIs	
CPU	μPD70008A-6 Code compatible with Z80
ROM	Maximum 256 KByte + 256 KByte (Memory card) Standard 256 KByte
RAM	Maximum 32 KByte + 256 KByte (Memory card + Optional) Standard 32 KByte Optional 128 KByte
Power consumption	80 mA (typ. at 6VDC)
Dimensions	1" (H) × 11-2/3" (W) × 8-2/7" (D) 25.4 (H) × 297 (W) × 210 (D) mm
Weight	2.42 lbs.(1.1kg) with batteries

I/O Interface

RS-232C

Conforms to EIA standard signal	TXD (Transmit Data) RXD (Receive Data) RTS (Request to Send) CTS (Clear to Send) DSR (Data Set Ready) DTR (Data Terminal Ready) CD (Carrier Detect)
Communications protocol	
Word length	5, 6, 7, or 8 bit
Parity	NONE, EVEN or ODD
Stop bit length	1, 1.5, or 2 bit
Baud rate	75, 110, 150, 300, 600, 1200, 2400, 4800, or 9600 bps (19200 bps: when used for the FDD)
XON/XOFF	Enable/Disable
CR/LF	CR/LF/CR + LF
XMODEM	ASCII/CRC-XMODEM
Maximum transmission distance	16.5 feet (5 meters)
Maximum driver output voltage	+5 volts and −8 volts
Maximum receiver input voltage	± 15 volts
Minimum receiver input voltage	± 3 volts

Printer interface

Conforms to Centronics interface standards	
Handshake signals	/STROBE, BUSY, /BUSY
Audio cassette interface	
Data transfer rate	1500 BPS (Mark 2400 Hz, Space 1200 Hz)
Input level	0.8 to 5 volts (peak-to-peak)
Output level	600 mV (peak-to-peak)

Expansion card interface

RAM card	32 KByte, 64 KByte, or 128 KByte
ROM card	Less than or equal to 256 KByte

II. DISASSEMBLY INSTRUCTIONS

II-1. Top Case

1. Remove 4 hexagon screws from the CN3/CN6 DSUB Connector.

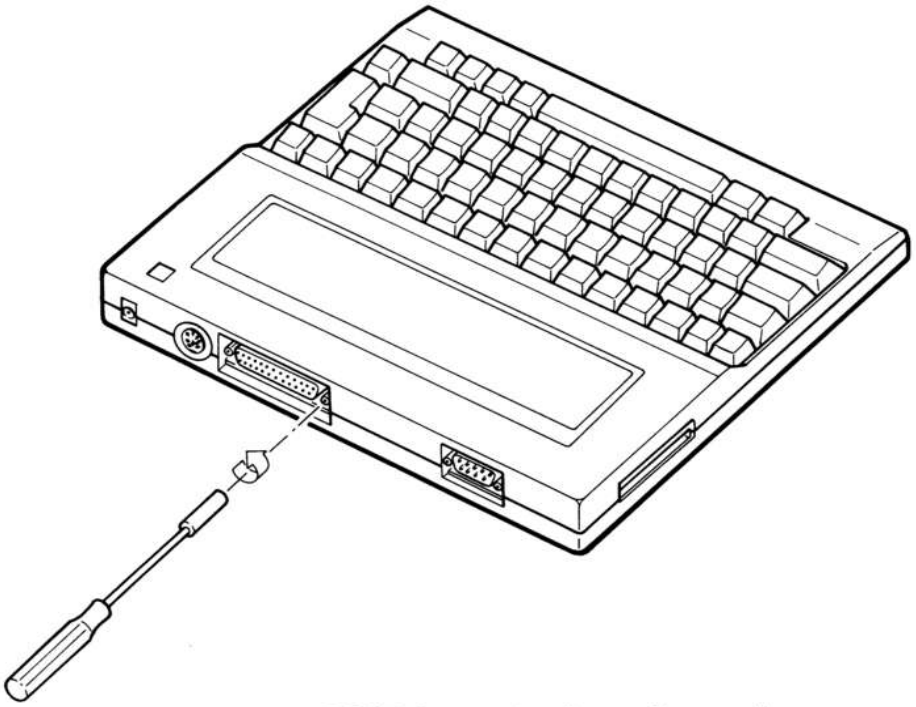


Figure 2-1. DSUB Connector Screw Removal

2. Remove the Main Batteries.

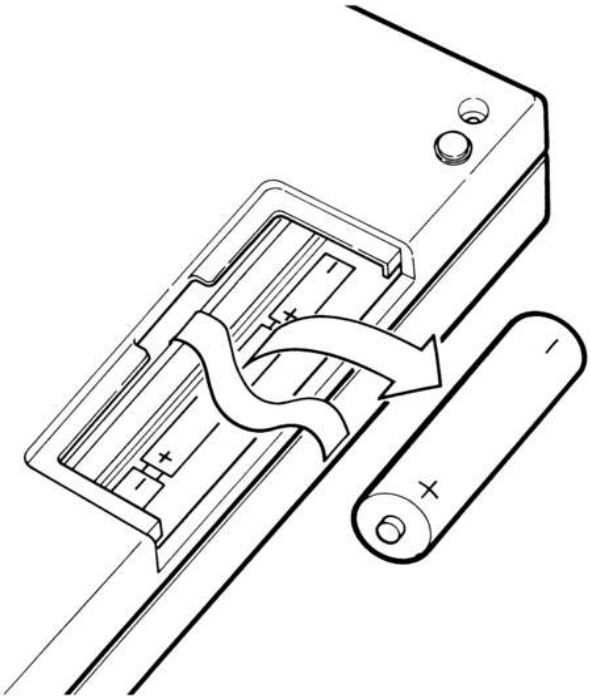


Figure 2-2. Removal of Main Batteries

3. Remove 5 screws "A" from the lower case.

4. Remove the upper case.
   The upper and lower cases are secured by snaps. Pull up the front of the upper case first, as shown below. Do not apply too much force when pulling it.

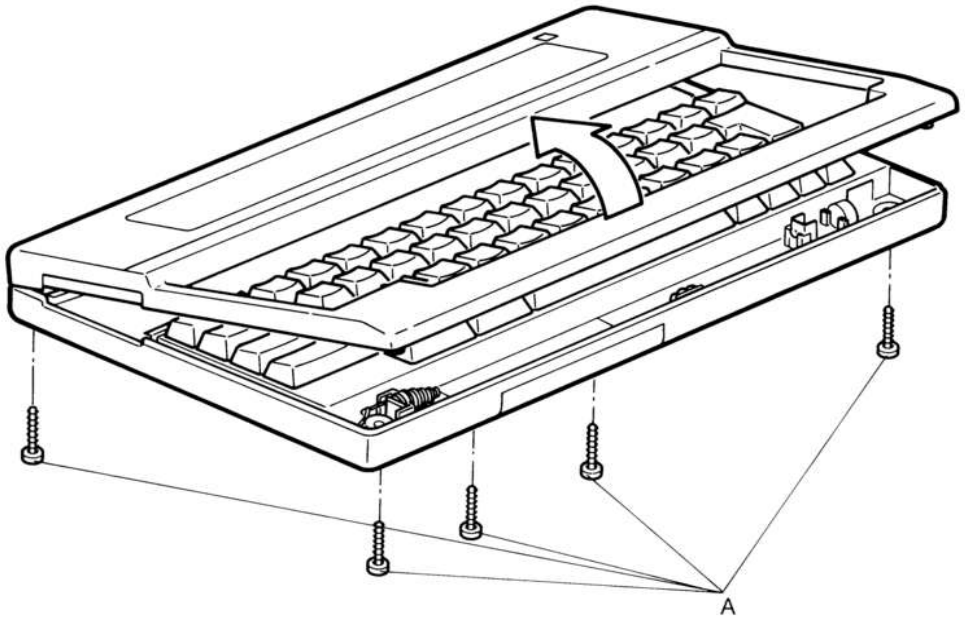


Figure 2-3. Top Case Removal

5. Disconnect the LCD flat cable from the connector on the main PCB.

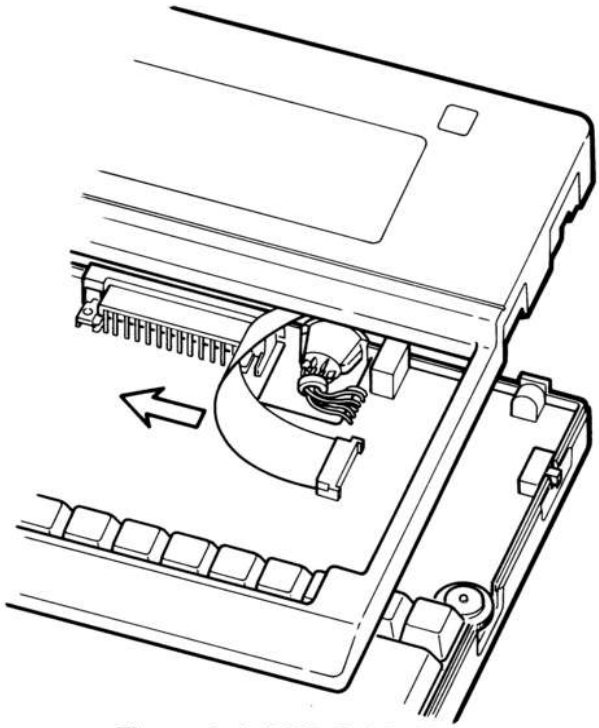


Figure 2-4. LCD Cable Removal

II-2. Keyboard

1. Remove 2 screws "B" securing the keyboard to the bottom case.
2. Disconnect the keyboard flat cable from the connector on the main PCB.
3. Remove the keyboard.

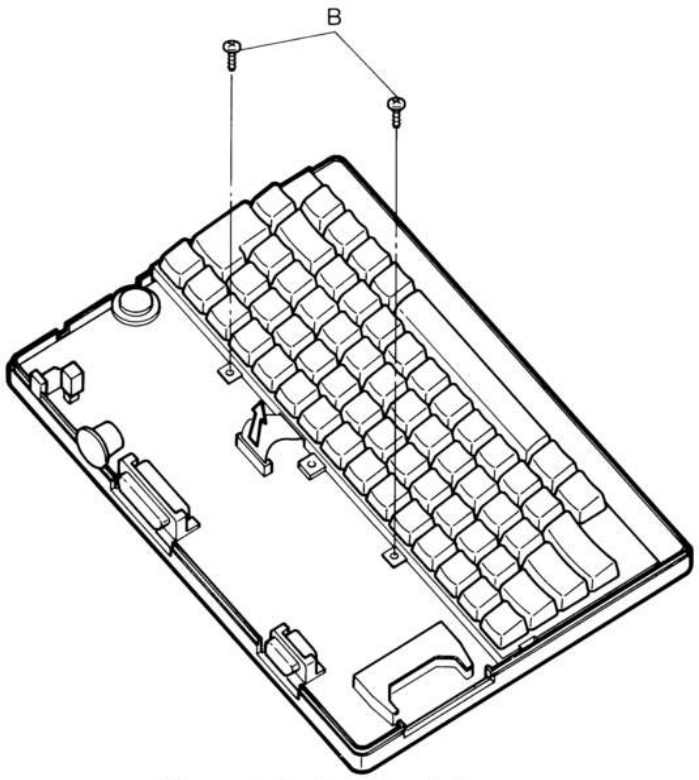


Figure 2-5. Keyboard Removal

II-3. LCD

1. Remove 4 screws "C" securing the LCD PCB to the upper case.

2. Remove the LCD PCB.

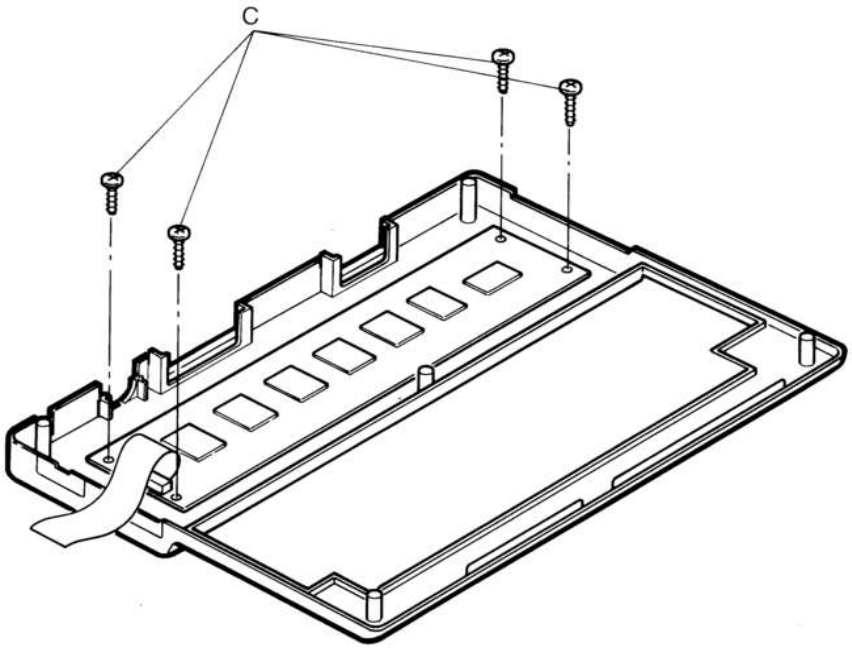


Figure 2-6. LCD Removal

II-4. Main PCB

1. Disconnect the flat battery cable from the connector on the main PCB.

2. Remove the five electric wires for the cassette connector using a soldering iron.

Wire assignment

1	Brown
2	Red
3	Orange
4	Yellow
5	Green

3. Remove 1 screw "D" securing the main PCB to the bottom case.

4. Remove the main PCB.

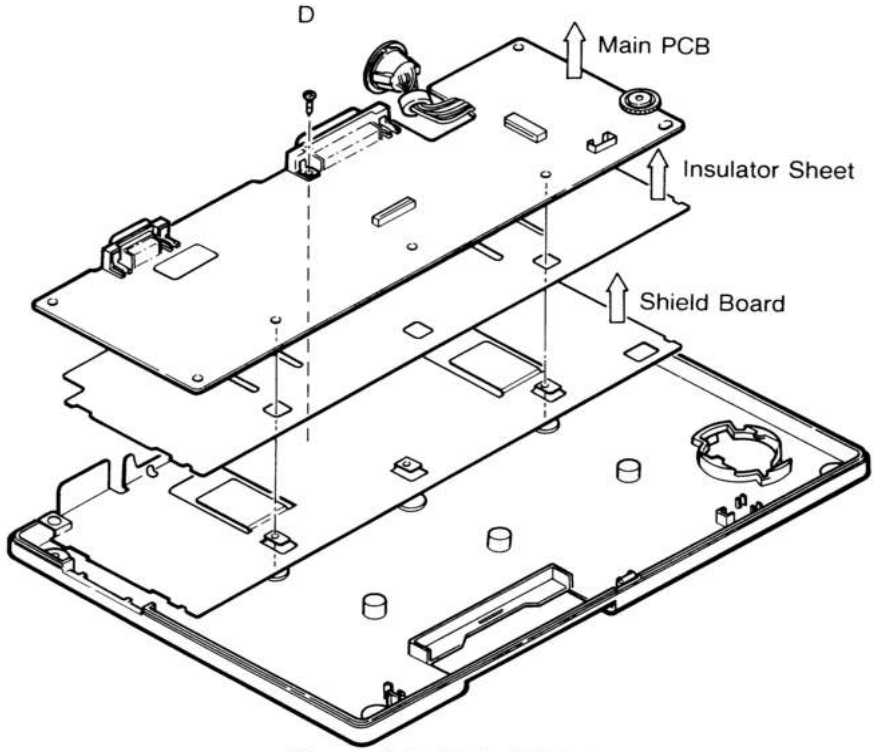


Figure 2-7. Main PCB Removal

5. Remove the insulator sheet.

6. Remove the shield board.

II-5. Sub PCB

1. Remove the back-up battery cover and the Lithium battery.

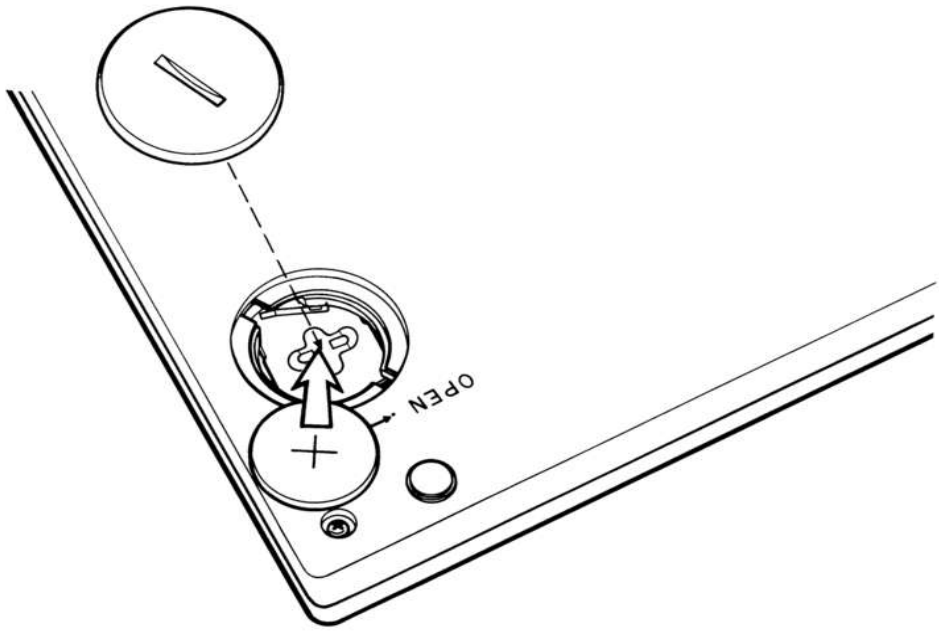


Figure 2-8. Back-up Battery Cover and Back-up Battery Removal

2. Remove the spring for the negative battery terminal.
3. Remove the main positive battery terminal.
4. Remove the buzzer.
5. Remove the sub PCB.

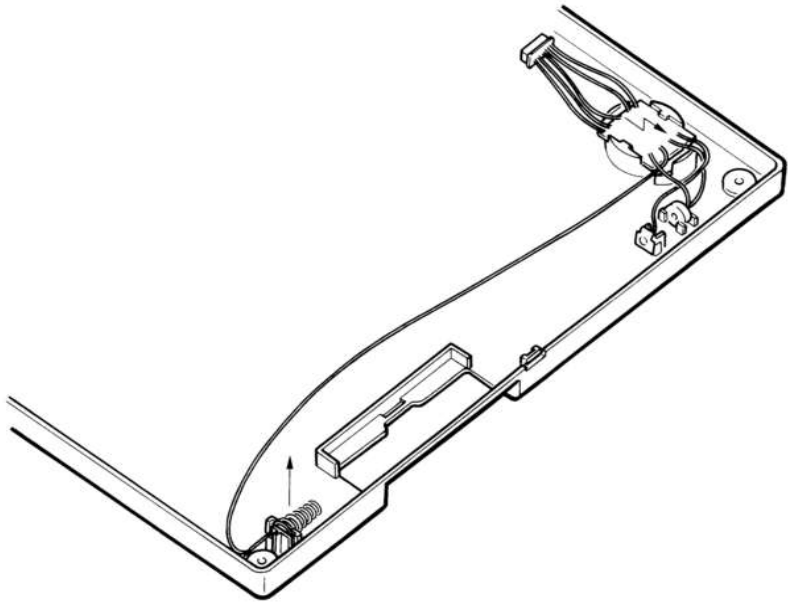


Figure 2-9. Lower Case View

III. MAINTENANCE

III-1. Clean the Case and LCD Display

1. To avoid operational trouble, always keep the Tandy WP-2 clean.

2. Clean the case and the LCD screen using a soft, dry, lint-free cloth.

3. For tough stains, clean the case or the LCD screen with "Freon" 113.

Caution: Do not use any solvents other than "Freon" 113.

Note: To retain the contents of RAM, turn on the protect switch. If you turn off the protect switch, the WP-2 will not turn on, even if you push the power switch.

IV. THEORY OF OPERATION

IV-1. Hardware Specifications

CPU		NEC μPD70008A-6
CPU CLOCK		5.5296 MHz
RAM		288 Kbyte (Maximum, internal + IC card)
		32 Kbyte (Standard)
	internal	32 Kbyte (Optional internal RAM)
		128 Kbyte (Optional internal RAM)
	IC card	32 Kbyte (Optional IC Card)
		64 Kbyte (Optional IC Card)
		128 Kbyte (Optional IC Card)
ROM		512 Kbyte (Maximum)
		256 Kbyte (Standard)
		32 Kbyte (Optional IC Card)
		64 Kbyte (Optional IC Card)
		128 Kbyte (Optional IC Card)
		256 Kbyte (Optional IC Card)
DISPLAY		
Control Device		MSM6255 LCD Controller
Graphic Resolution		480 × 64 dots
Character Display		80 characters × 8 lines
Display Device		Super twist nematic LCD panel
Video RAM		3840 bits
Effective Display Area		211.17 × 28.13 mm
		Dot size 0.41mm × 0.41 mm
		Dot pitch 0.44mm × 0.44 mm
		Aspect 1 : 1
KEYBOARD		
Number of Keys		62 keys (8 × 8 key matrix)
RS232C INTERFACE		
Standard		Conforms to EIA Standard
Device		μPD71051GU
		DS14C88 and DS14C89AN or SN75C188 and SN75C189AD
Word Length		5, 6, 7, or 8 bits
Parity		Even, Odd, or None
Stop Bit Length		1, 1.5, or 2 bits
Baud Rate		75, 110, 150, 300, 600, 1200, 2400, 4800, 9600, (19200 when used for the FDD)
Output Signal Level		Output signal base on +5V and −8V
Input Signal		Voltage SPACE = +3V to +15V
		MARK = −3V to −15V
PRINTER INTERFACE		
Control		The printer is controlled by the STROBE and BUSY signals.
Output		When a printer is used, the connector can be plugged in or removed without destroying the inner circuits of the device regardless of power ON/OFF. In addition, the interface circuits can effectively withstand static discharge breakdown.

AUDIO CASSETTE INTERFACE

Data Rate	1500 BPS (Mark = 2400 Hz, Space = 1200 Hz)
Input Level	0.8 to 5 volt (peak-to-peak)
Output Level	600 mV (peak-to-peak)

MEMORY CARD INTERFACE

Using Model	TOSHIBA MEMORY CARD

POWER SOURCE	Output(DC): +5V 160mA, −8V 12mA, −15V 10mA
Main Battery	6V, four AA size Alkaline batteries or 4.8V, 450mAh, four AA size Nickel-Cadmium batteries
Back-up Battery	3V, 270 mAh flat Lithium battery This battery is used to hold the data of the main RAM and the expanded internal RAM.
Battery Votage Warning	The warning is indicated by "LOW BATTERY" on the screen and one beep. The user is instructed to change the batteries when the voltage goes below 4.0 V(Alkaline) or 4.7 V(Ni-Cd). After the warning, the system can be used for about 10-30 minutes.
Back-up Warning	The warning is indicated by "LOW BACKUP" on the screen and one beep. Then, the screen turns on and off. The user is instructed to change the battery when the voltage goes below 2.3 V. Before changing a back-up battery, save all RAM (standard and internal expansion) data to another device(s), or the system loses all RAM data.

Block Diagram

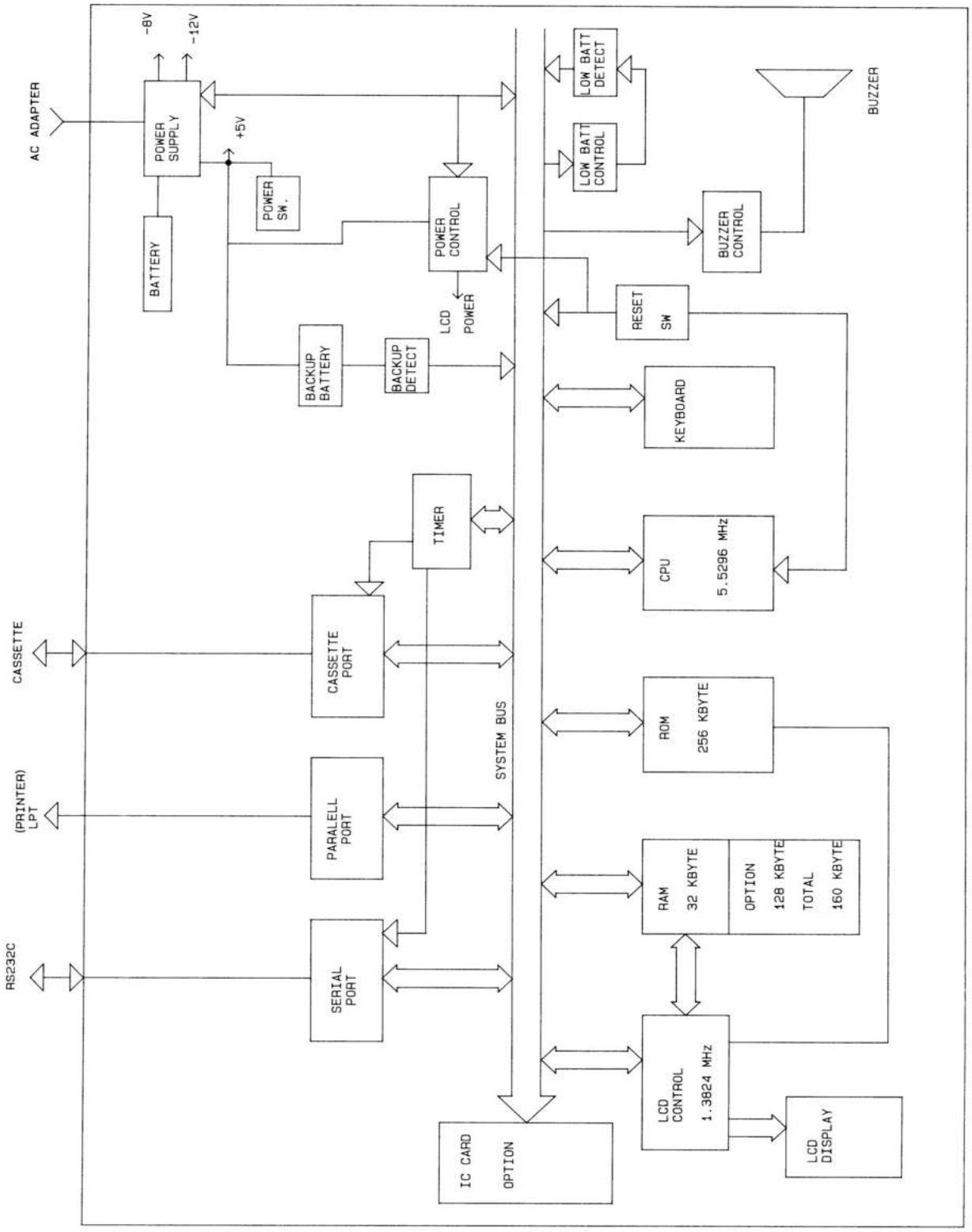


Figure 4-1

IV-4. Memory Map

The Memory Map is shown in Figure 4-2. Expansion RAM is mapped on the I/O address.

ROM: Expandable 16 KByte each
RAM: Expandable 32 KByte each

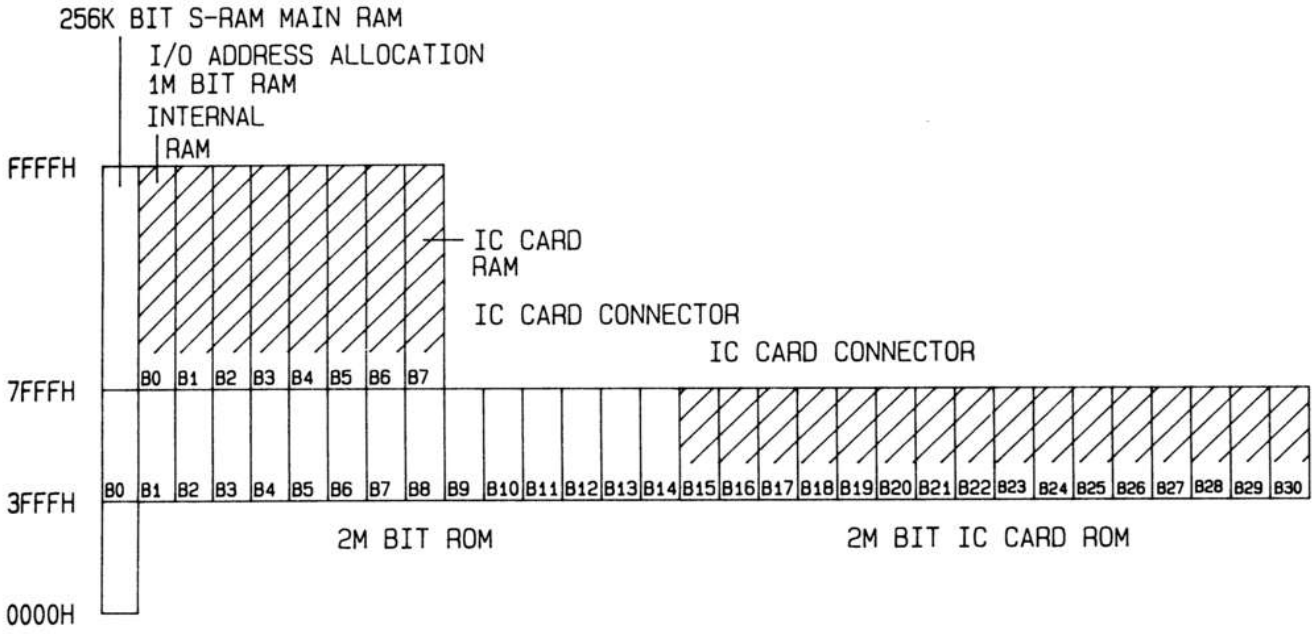


Figure 4-2

IV-5. Main RAM Control Circuit

Figure 4-3 shows the LCDC DIEN and the CPU $\overline{\text{WAIT}}$ control diagram. The Tandy WP-2 uses VRAM and MAIN RAM in common on a piece of RAM. To do this, the Tandy WP-2 uses synchronous accessing by the DIEN signal. The Tandy WP-2 avoids collision of CPU accessing and LCD refresh by waiting for CPU. Both the DIEN signal and WAIT signal are generated in IC5.

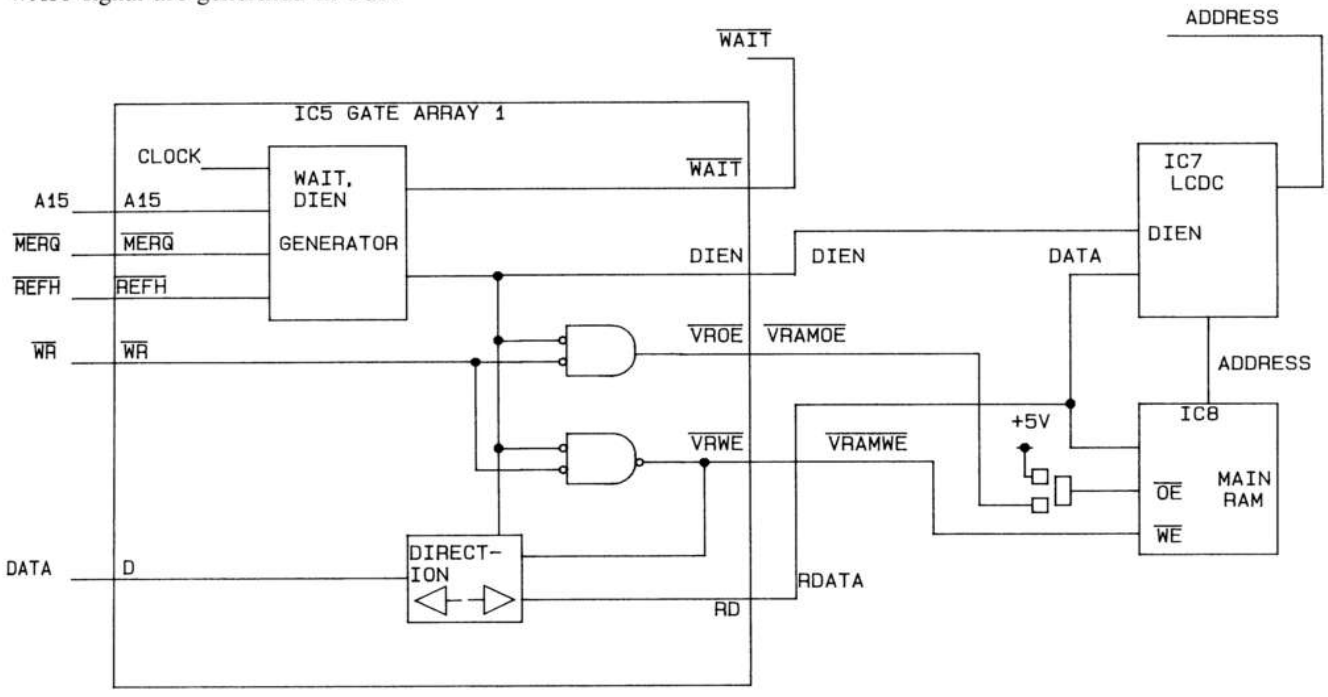


Figure 4-3

IV-6. Expansion RAM Control Circuit

Figure 4-4 shows the selecting bank diagram for the expansion RAM.
Bank 0-3 is used by the internal expansion RAM, and bank 4-7 is used by the IC card RAM.
Figure 4-4 shows the expansion RAM read/write diagram.
Both the selecting bank signal and read/write signal are generated in IC5. RAM bank control I/O is in bits 5-7 of 51H.

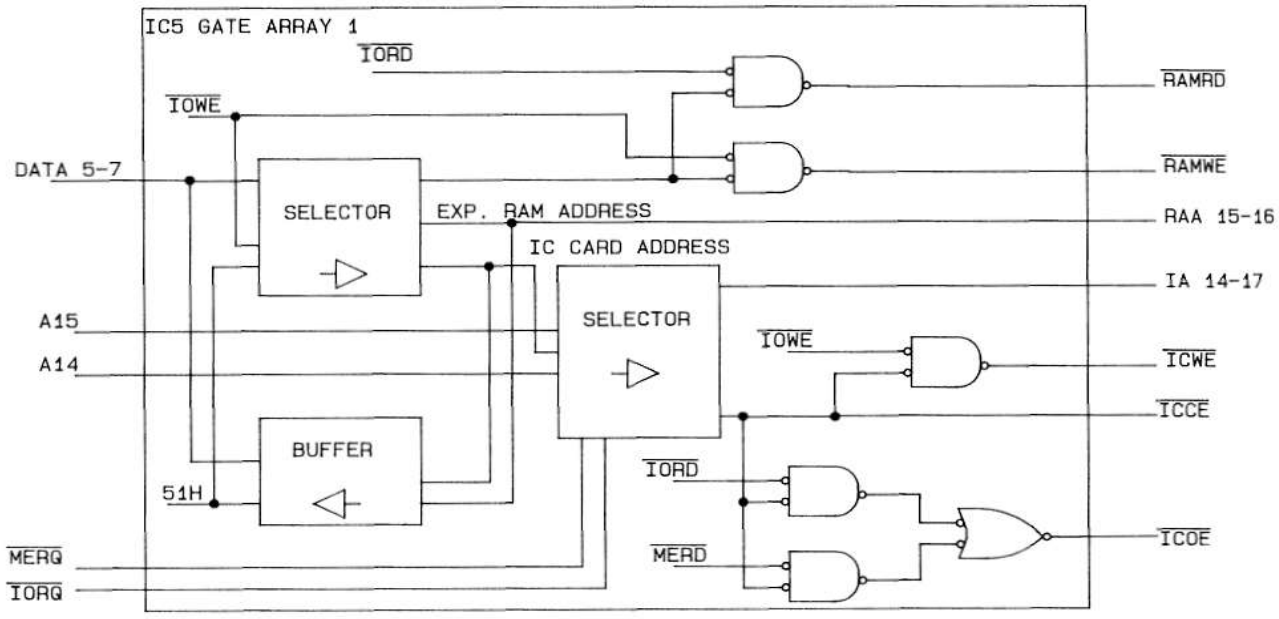


Figure 4-4

IV-7. ROM Control Circuit

Figure 4-5 shows the selecting bank diagram for the ROM. Accessing address 0-3FFF is not used in the selecting bank circuit. Bank 0-14 is used by the standard ROM, and bank 15-30 is used by the IC card ROM.
ROM bank control I/O is in bits 0-4 of 51H.

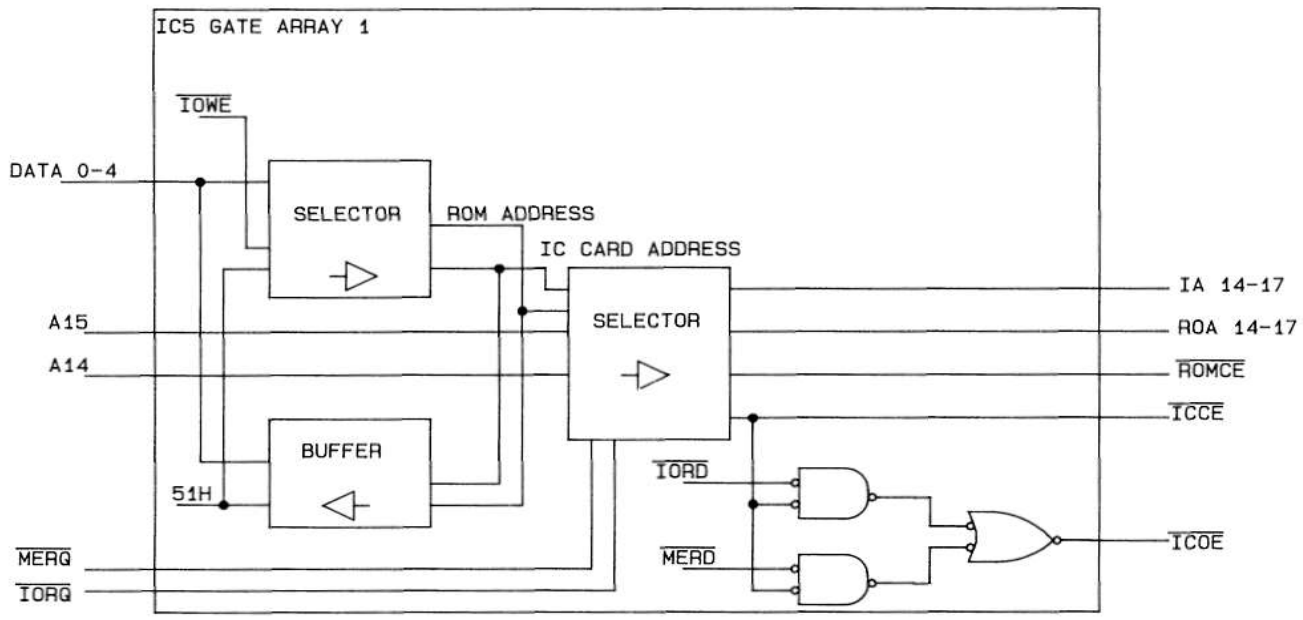


Figure 4-5

IV-8. I/O Address Map

ADDRESS		BIT CONTENTS	CONTROL
00H		Key scan data	Read/Write
UART CONTROLLER			
10H		82C51 character data	Read/Write
11H		82C51 control/status data	Read/Write
TIMER			
20H		Timer counter 0	Write only
21H		Timer counter 1	Write only
22H		Timer counter 2	Write only
23H		Timer control word	Write only
PRINTER			
30H		Printer data out port	Write only
31H	bit7	Printer strobe out port	Write only
32H	bit0	Printer Busy read port	Read only
32H	bit7	Printer /Busy read port	Read only
INTERRUPT/NMI CONTROL			
		(setting interrupt mask control)	
50H	bit0	Timer counter 0	0/ON, 1/OFF
	bit1	Serial RXRDY	0/ON, 1/OFF
	bit2	Low battery	0/ON, 1/OFF
	bit3	External interrupt	0/ON, 1/OFF
		(setting NMI mask control)	
	bit4	DC/DC power off	0/ON, 1/OFF
	bit5	Back-up battery low	0/ON, 1/OFF
		(showing interrupt status)	
50H	bit0	Timer counter 0	0/ON, 1/OFF
	bit1	Serial RXRDY	0/ON, 1/OFF
	bit2	Low battery	0/ON, 1/OFF
	bit3	External interrupt	0/ON, 1/OFF
		(showing NMI mask control)	
	bit4	DC/DC power off	0/ON, 1/OFF
	bit5	Back-up battery low	0/ON, 1/OFF
MEMORY BANK CONTROL			
51H	bit0-4	Write/Read select ROM bank number	
	bit5-7	Write/Read select RAM bank number	
SYSTEM STATUS REGISTER			
		(Write Register)	
52H	bit0	DC/DC power control	0/ON, 1/OFF
	bit1	Beep control	0/OFF, 1/ON
	bit6	LCD power control	0/OFF, 1/ON
	bit7	Main battery select	0/Ni-Cd, 1/Alkaline
		(Read Register)	
52H	bit0	Power switch show	0/ON, 1/OFF
	bit1	Beep status show	0/ON, 1/OFF
	bit2	RS232C CD status	0/ENABLE, 1/DISABLE
CASSETTE CONTROL			
		(Read port)	
53H	bit0	Read output data	
	bit7	Read input data	
		(Write port)	
53H	bit7	Timer counter 1 set	0/DISABLE, 1/ENABLE
54H	bit0	Remote motor control	0/OFF, 1/ON

ADDRESS	BIT CONTENTS	CONTROL
6255 (LCDC) CONTROL		
60H	Read/Write port	
61H	Instruction register port	

IV-9. Interrupt

The μPD70008A-6 has abundant interrupt processing functions:
External interrupt: $\overline{\text{NMI}}$ (Non-maskable interrupt)
$\overline{\text{INT}}$ (Maskable interrupt)
Interrupt by software
Interrupt control list: Timer counter
Serial RXRDY
Low battery

There are two NMI-interrupt sources in the Tandy WP-2.

1. DC/DC off
2. Low Back-up Battery

DC/DC OFF is a signal for emergency power off. The DC/DC becomes active when the power supply is stopped. When this signal becomes active, register, bank number and interrupt information are saved by software.
Low back-up battery is a signal for back-up battery voltage warning. The low back-up battery signal becomes active when the back-up battery voltage goes down to 2.3V. The low back-up battery signal is maskable by the I/O port 50H.

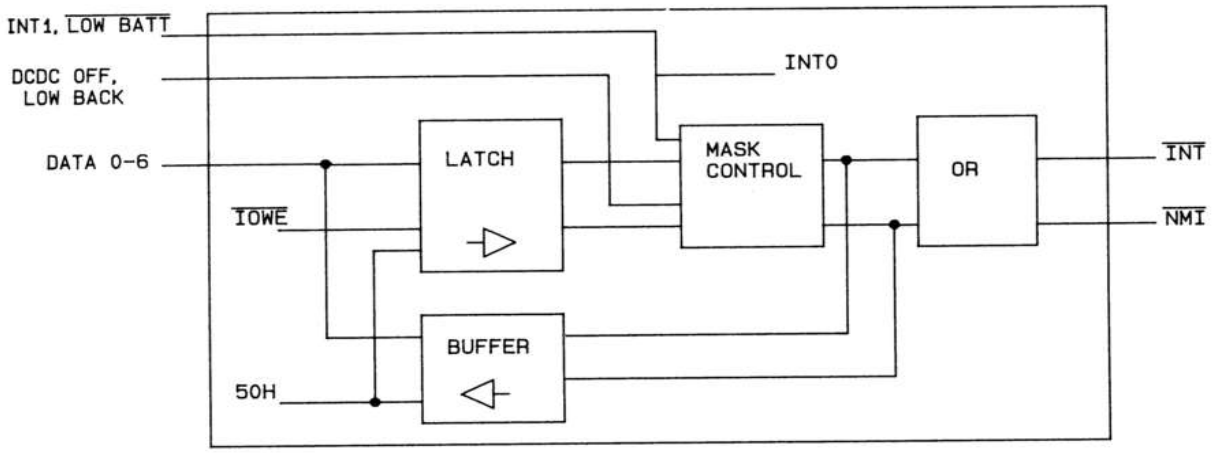
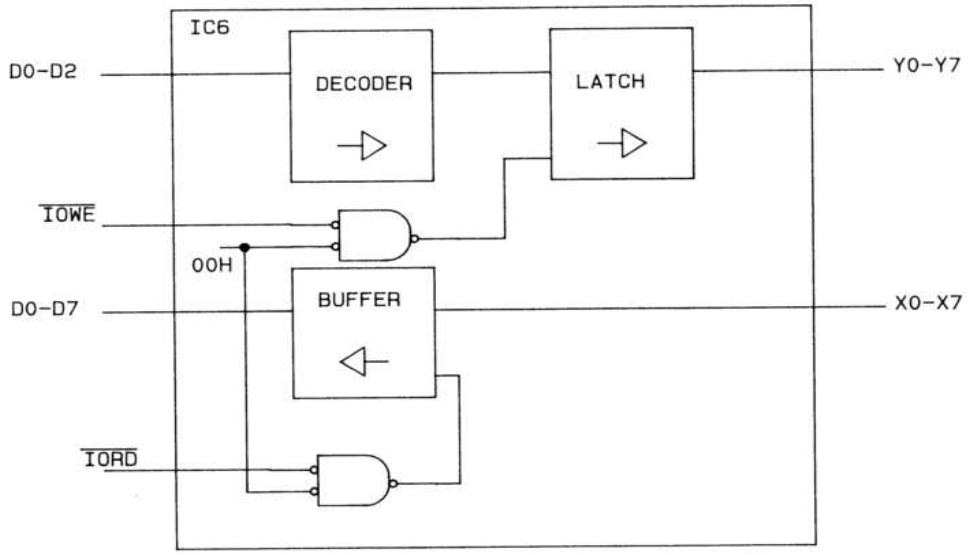


Figure 4-6

IV-10. Keyboard

The Tandy WP-2 uses an internal keyboard.
Key strobe signals are emitted from the Y0 to Y7 terminals of IC6. The return signals from the keyboard pass through the X0-X7 terminals of IC6 and are sent to the CPU. Figure 4-7 shows the block diagram in IC6.



IV-11. Cassette Interface Circuit

The cassette interface circuit is subdivided into three sections:

Write Circuit

Transmits data output through the CTD terminal of IC6. The output voltage level is reduced by R14 and R15. The data goes to a cassette recorder's MIC jack. When bit 7 of I/O port 53H is "H", the RXC clock outputs from the CTD terminal.

Read Circuit

The signal input from the earphone jack of the cassette recorder passes through C12, and then is input to the comparator circuit consisting of IC14. The signal is converted into a digital signal and is sent to the CRD terminal of IC6. The control I/O is in bit 0 of 53H.

Remote Circuit

As a result of writing data "1" into bit 0 of I/O port 54H, the CRY signal is changed to H level.
Then, TR2 is switched on and relay RE1 is energized, closing the relay contacts. This causes the drive motor of the cassette recorder to operate.

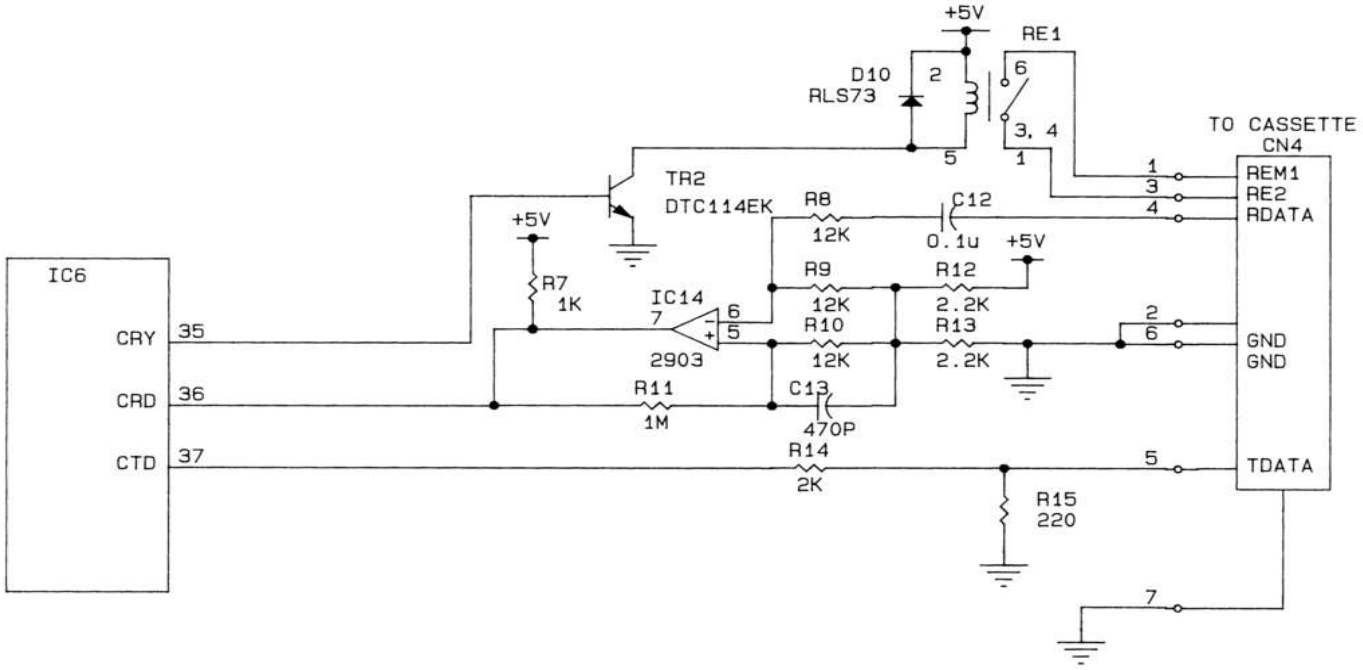


Figure 4-8

IV-12. Printer Interface Circuit

The printer interface circuit conforms to Centronics standards. Figure 4-9 shows the printer interface circuit.
The BUSY signal from the printer is read from the BUSY signal of IC6. If the condition is not busy (BUSY="L"), the 8-bit parallel data is sent to the printer.
As soon as the printer receives the /PSTB signal, the BUSY signal changes to H, indicating that the printer is busy. The CPU then waits for a while until this BUSY signal becomes "L". The printer prints the one character corresponding with the 8-bit parallel data. After completion of the one character printing, the printer sets the BUSY signal to "L". Then, CPU sends the next 8-bit parallel data. If the printer is ON LINE, the /BUSY signal is H and sent to the CPU, passing through the /BSYB signal of IC6. However, when the printer is OFF LINE, the /BUSY signal is L, and transmission of print data to the printer is inhibited by the CPU.
Printer control I/O is in 30H, 31H and 32H.

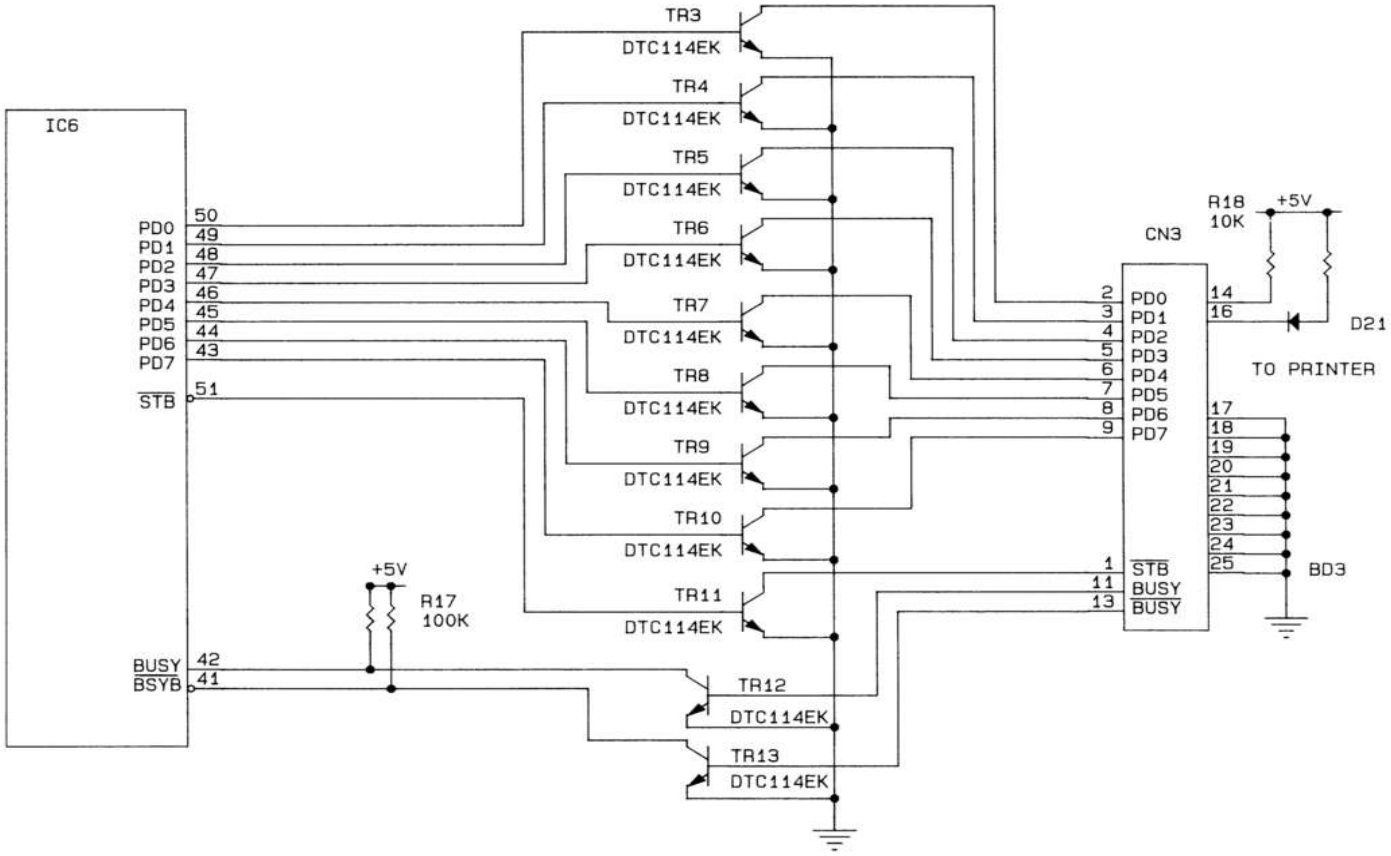


Figure 4-9

IV-13. Serial Interface Circuit

Figure 4-10 shows a block diagram of the serial interface.
Serial data for the Tandy WP-2 is controlled by UART(μPD71051) and IC5. The UART(IC9) performs serial-to-parallel conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, or framing).
Figure 4-10 shows the pin layout definitions of UART.

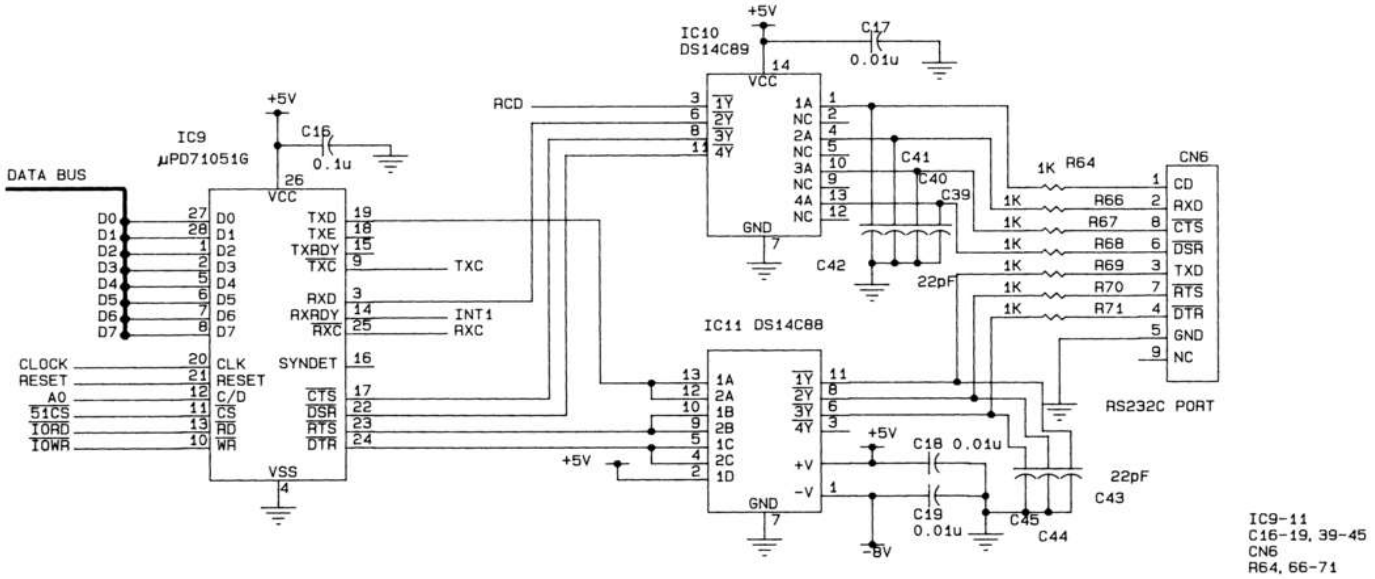


Figure 4-10

IV-14. Buzzer Control Circuit

The system unit has a 12 mm buzzer. The buzzer driver is capable of about 0.1 watts of power. If bit 1 of I/O port 52H becomes "H," then the BEEP of IC6 becomes "H" and the buzzer rings. The buzzer sounds by repeated switching of the buzzer driving transistor. This is caused by H,L,H,L... output signals from the BEEP synchronized with the frequency for sounding the buzzer.

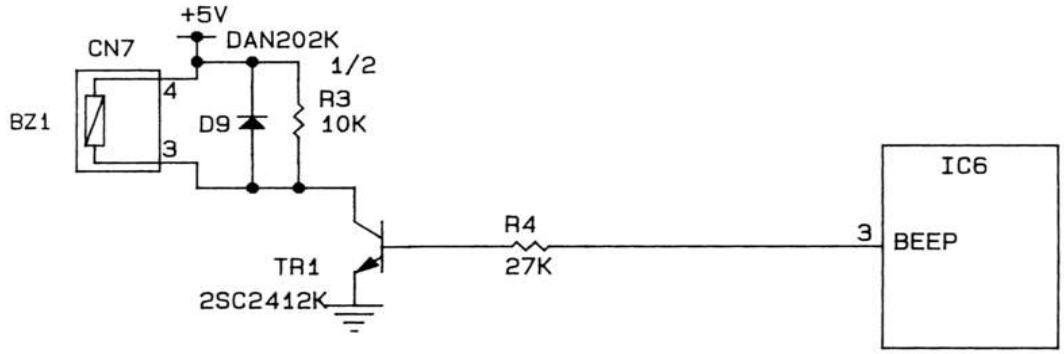


FIgure 4-11

IV-15. LCD Controller

CPU interface

The CPU interface circuit of the MSM6255 is shown in Figure 4-12.

Data Bus (D0-D7), Address Bus (A0-A15), /LCDCS, /IORD, /IOWR, and DIEN serve as the interface between the CPU and MSM6255.

When the DIEN signal is "H", LCDC accesses the main RAM. The CPU accesses the main RAM when the DIEN signal is "L."

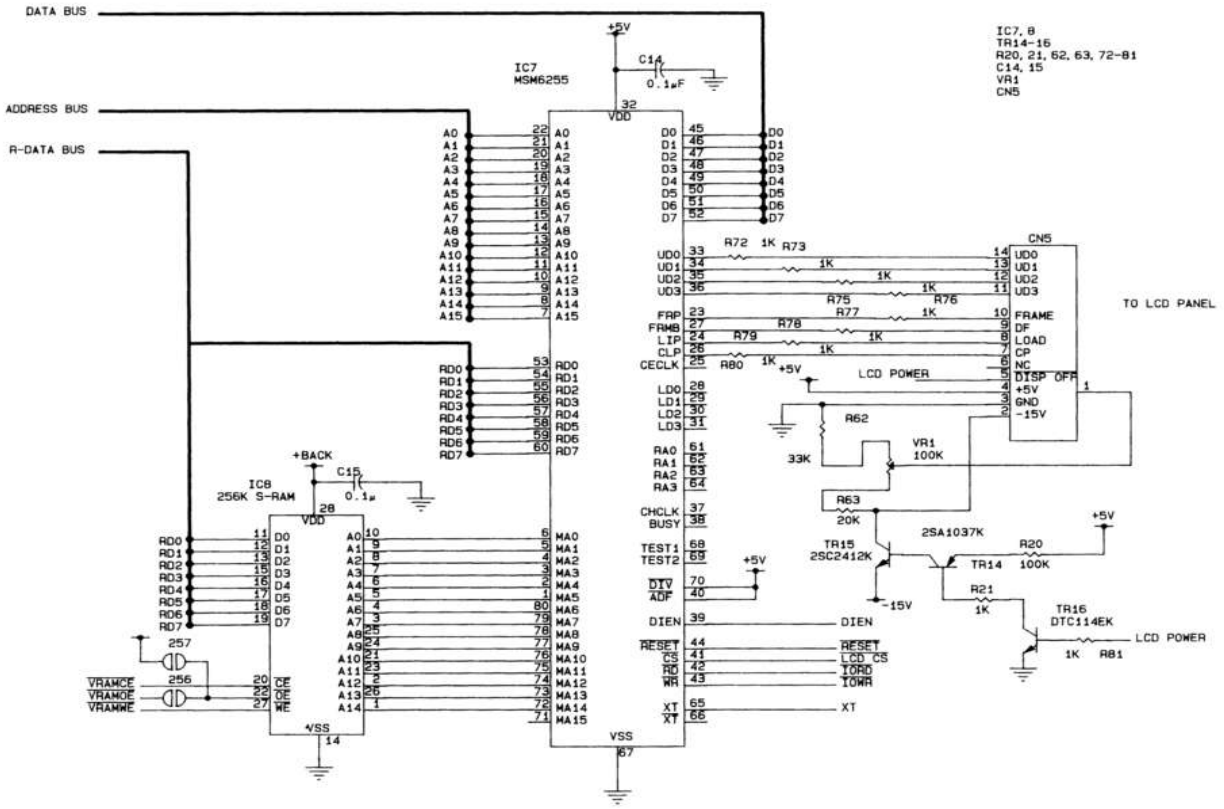


Figure 4-12

IV-16. Power Supply

The system DC power supply has an approximately 1.2 watt, 3 Voltage-level regulator. It is integrated into the system unit, and supplies power for the system unit, and IC Card.
The supply provides 160mA +5VDC +/−5%, 12mA −8VDC +/− 10% and 10mA −15VDC +/− 10% at 6VDC.
The system unit takes approximately 50 to 140 mA of +5VDC.
The −8VDC is used for powering the Electronic Industries Association (EIA) drivers for communications in the main PCB. The −15VDC level is used for LCD bias.

+5VDC Output Voltage Circuit
This is a one-transistor self-excited DC/DC converter, which is called R.C.C. (Ringing Choke Converter). Figure 4-13 shows the principle of the circuit.

(a) When the power is supplied to VI(B+), Tr turns on and current (Ic) flows through the primary winding of the transformer.
With this current, voltage (Vb) is induced to the base winding, then Tr immediately reaches saturation.

(b) Tr can no longer maintain saturation. Therefore, Tr is turned off immediately. Then voltage Vo is created by the magnetic energy stored in the transformer, and the voltage is sent to output Vo through the diode D.

(c) When the energy stored in the transformer is discharged, the output current (ID) diminishes and reaches zero. However, Tr turns on immediately with the base voltage Vb which is induced from the primary winding, and the above actions are repeated.

The operation of the blocks of the +5V Power Supply circuit is as follows. (Refer to Figure 4-14.)

Block 1 The block operates like a boot-up resister Rs in Figure 4-13. The block is made of a boot-up circuit, output voltage controller, and shut-down circuit, and the block controls TR30.

Block 2 This switching transistor operates like a transistor in Figure 4-13.
Block 3 This transformer generates +5VDC, −8VDC, and −15VDC output voltages.

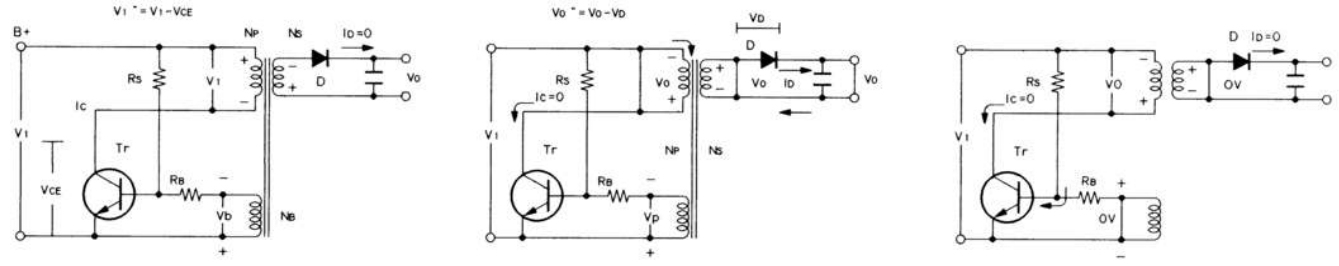


Fig. 4-13

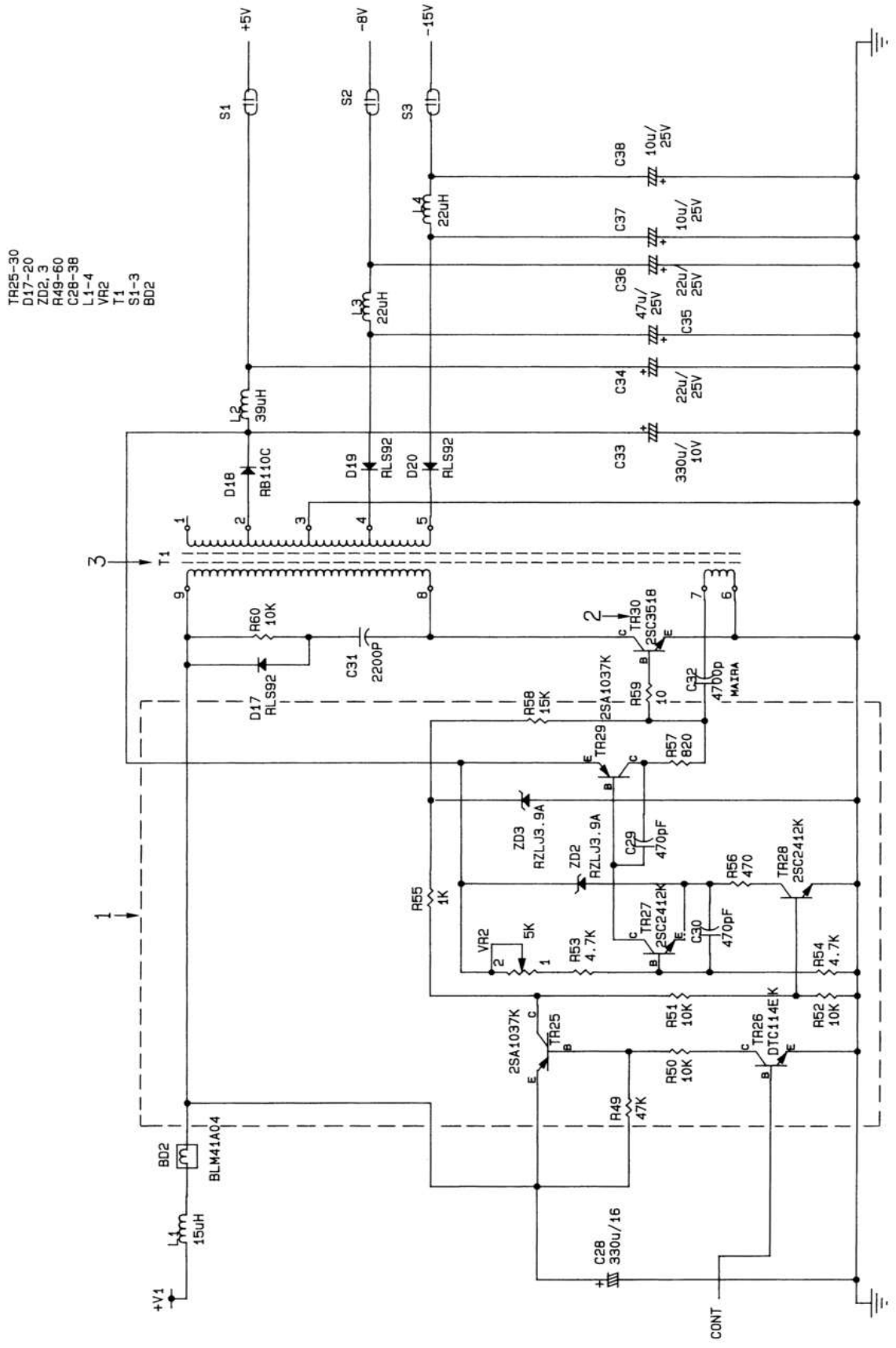

TR25-30
D17-20
ZD2, 3
R49-60
C28-38
L1-4
VR2
T1
S1-3
BD2
+5V
-8V
-15V
S1
S2
S3
C38 10u/ 25V
C37 10u/ 25V
C36 47u/ 25V
C35 22u/ 25V
C34 22u/ 25V
C33 330u/ 10V
L4 22uH
L3 22uH
L2 39uH
D18 RB110C
D19 RLS92
D20 RLS92
T1
R60 10K
C31 2200P
D17 RLS92
TR30 2SC3518
R58 15K
2SA1037K
R59 10
C32 4700p MAIRA
TR29
R57 820
ZD3 RZLU3.9A
ZD2 RZLU3.9A
C29 470pF
R56 470
TR28 2SC2412K
R55 1K
VR2 5K
R53 4.7K
TR27 2SC2412K
C30 470pF
R54 4.7K
2SA1037K TR25
R51 10K
R52 10K
TR26 DTC114EK
R50 10K
R49 47K
BD2
BLM41A04
L1 15uH
C28 330u/16
+V1
CONT

Figure. 4-14

IV-17. Software Calls

Software calls are supplied on MEMORY CARD (ROM IC CARD) or files.

ROM PROGRAMS

The applications on the ROM IC CARD can be executed from WORDPROCESSOR. Execute it by pressing the key combination of 'F2' and '7.' The return to the WORDPROCESSOR is designed by the application side.

RUN FILES

The RUN FILE can be executed from FILES. Execute it by pressing the key combination of 'F2' and '7' after selecting the file. The return to FILES is designed by the application side. This type of application can be kept in memory as a Driver or Filter such as a handler of key scan.

(Sample of program)

This program can execute on the WP-2 system.

```
ON-ROM          EQU     0               ; FLAG OF COMPILER
CLS             EQU     011EH           ; ENTRY OF BIOS TO CLEAR LCD
GETCH           EQU     0103H           ; TO GET KEY
PUTCH           EQU     01A3H           ; TO DISPLAY
BKSP            EQU     08H             ; CODE OF BACK SPACE

IF ON-ROM                               ; HEADER OF ROM APPLICATIONS

ORG     4000H
        DB      'PI'                    ; ID
        DW      0                       ; RESERVED
        DB      15                      ; BANK OF ENTRY
        DB      START                   ; ADDRESS OF ENTRY
        DW      0                       ; RESERVED

ELSE
                                        ; HEADER OF RUN FILES
ORG     0AC00H-8
        DB      'PR'                    ; ID
        DW      PRGEND-PRGTOP+1         ; SIZE OF PROGRAM
        DW      START                   ; ADDRESS OF ENTRY
        DW      0                       ; LOCATED ADDRESS (HERE IS 0)
```

The WP-2 cannot handle a RUN FILE unless it has an identification header. The format for this ID header is as shown in the sample program above. The LOCATED ADDRESS in the ID header is "0000H." The WP-2 reads the main part of a program following the ID header into the area beginning at "AC00H" and places the control on the address designated as the ADDRESS OF ENTRY.

There are times when a loaded RUN FILE reads SUB RUN FILEs and allows them to run. The LOCATED ADDRESS and ADDRESS OF ENTRY in a SUB RUN FILE's ID header are determined by the root RUN FILE and are registered accordingly. The contents of the ID header for the SUB RUN FILEs are different from those of a root RUN FILE. The WP-2 handles only certain RUN FILEs; therefore, a user cannot execute a SUB RUN FILE without a root RUN FILE. Also, the WP-2 does not have a program loader for SUB RUN FILEs; the root RUN FILE must have a program loader.

```
ENDIF

PRGTOP:                                 ; TOP OF PROGRAM
START:                                  ; PROGRAM BEGINS FROM HERE
        CALL    CLS                     ; CLEAR THE SCREEN
        CALL    GETCH                   ; GET THE DATA FROM CONSOLE
        LD      A,H

        BIT     0,L                     ; IF 'EXIT' KEYS ARE PRESSED,
        JR      Z,DISPLAY               ; RETURN TO WP-2 SYSTEM.
        CP      BKSP
IF ON-ROM
        RET     Z
ELSE
        XOR     A                       ; RETURN WITH FLAG
        RET
ENDIF
```

The RETURN WITH FLAG means that program area is returned to the system. If it needs to keep the program as a Driver or Filter, register "A" must be set to FF.

```
DISPLAY:
        CALL    PUTCH   ; INDICATE ONE CHARACTER
        JR      START   ; TRY AGAIN.

PRGEND:                 ; END OF PROGRAM

END
```

You can get the hex file to compile the source program such as the one shown above. However, you need to record the program into a ROM or RAM IC CARD for the WP-2 to operate it. If the program is a ROM APPLICATION, you burn the program into the ROM. If the program is a RUN FILE, it is better if you transfer the program through XMODEM. Of course, you must convert the file to binary data.

IV-18. Software and Hardware Memory Map

MEMORY MAP

The RAM DISK is assigned to the I/O port from bank 0 to bank 3. The MEMORY CARD is assigned to the I/O port from bank 4 to bank 7. Each bank begins at address 8000, and ends at address FFFF.

All system's applications are included in the MAIN ROM. It begins at address 0000 in bank 0, and ends at address 7FFF in bank 14. From bank 15 to bank 30 is the area of IC card ROM APPLICATIONS. Bank control I/O is in port 51H.

DETAILS OF PROGRAM

Bank	Address	Contents
[ROM] : body of programs		
0	0000-23FF	BIOS jump table, and program of BIOS
0	2400-2BFF	Character font set
0	2C00-2FFF	Interface of function of dictionary, and handler
0	3000-	WORDPROCESSOR
1	-73FF	
1	7400-	Dictionary
14	-7FFF	
[RAM] : work area		
—	8000-833F(+512+320)	SPELLER work area
—	8340-8344	Hook table of SPELLER
—	8345	Hook table for TIMER interrupt
—	8348	for key scan into timer int.
—	834B	for character out to console
—	834E	for debugger
—	8351	for external interrupt
—	8354	for RS-232C receive interrupt
—	8357-98FF	BIOS work area Editor (word processor) work area
	8357	Cursor's line (Y) position
	8358	Cursor's column (X) position
	835A	Pointer to store the key code
	835C	Pointer to get the code from buffer
	835E-83DD	Key buffer First byte (status bit) bit 0 : F2 key status bit 1 : F1 key bit 2 : Ctrl key bit 3 : Shift (right) key bit 4 : Shift (left) key bit 5 : Caps lock On/Off bit 6 : 0:GRPH/1:CODE mode bit 7 : 0:Normal/1:above mode Second byte (data) Data of key code. If mode is GRPH or CODE, this data is added at 20H.
	83FF	Value of counting the timer int.
	8403	Console controller status bit 0 : cursor brink ON/OFF bit 1 : type of cursor bit 2 : brink Enable/Disable bit 3 : character attribute
	840D	Pointer to store the receive data
	840F	Pointer to get the data from buffer
	8411-8510	Receive data buffer First byte (status bit) bit 0 : Flag, 0:no data/1:data

		bit 5 : Flaming error bit 6 : Overrun error bit 7 : Parity check error Second byte (data) Receive Data
—	9900-A7FF	LCD (VRAM area)
—	A800-ABFF	Stack area
—	AC00-FFFF	APPLICATION work area (Data of document, file or paste buffer)

HANDLER OF TIMER INTERRUPT

To handle the TIMER interrupt, the following must be done.

1) Refer to hook table of timer interrupt.

2) Initialize the TIMER device.

3) Power Switch status is checked and handled.

4) Control the LOW BATTERY indication.

5) Control the LOW BACK UP indication.

6) Auto Power Off control

7) Refer to hook table of key scan.

8) Handle the key scan.

If you want to change the Key Scan Handler of the WP-2 to another handler, you need to design the other Key Scan Handler as a RUN FILE PROGRAM. The initialize routine must rewrite the hook table to hook the other handler; that is, the entry address of the handler is written from the second byte in the hook table, and the instruction code for jump command is written into the first byte. The instruction 'POP' must be included in the handler routine as a dummy to ignore the handler of the WP-2.

HOOK TABLE OF DEBUGGER

To refer the hook table of the Debugger, execute the instruction 'RST 28H'. It will be used by the BREAK function to set the instruction 'RST 28H' to the address of the break pointer.

IV-19. IC Card

Pin Connection

Pin	Symbol
1	GND
2	/DET
3	CE2
4	/CE1
5	/OE
6	D0
7	D1
8	D2
9	D3
10	D4
11	D5
12	D6
13	D7
14	GND
15	NC
16	NC
17	A17
18	A16
19	A15
20	A14
21	A13
22	A12
23	A11
24	A10
25	A9
26	A8
27	A7
28	A6
29	A5
30	A4
31	A3
32	A2
33	A1
34	A0
35	R/W
36	NC
37	BCHK
38	VDD

Note / DET Signal

RAM Card: GND
ROM Card: NC

Pin Names

Symbol	Pin Name
A0-A17	Address Input
D0-D7	Data Input/Output
/CE1	Chip Enable Input 1
CE2	Chip Enable Input 2
R/W	Read/Write Control Input
/OE	Chip Enable Input
/DET	Card Detect
BCHK	Battery Voltage Check
VDD	Power (+5V)
GND	Ground
NC	No Connection

Operation Modes

Mode	/CE1	CE2	/OE	R/W	D0-D7	Power
Write	L	H	*	L	IN	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	Hi-Z	Standby
Standby	*	L	*	*	Hi-Z	Standby
Output Disable	L	H	H	H	Hi-Z	Active

Note: Hi-z means high-impedance. *: H or L

RAM CARD

Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Power Supply Voltage	0-7	V
VIN	Input Voltage	0-VDD	V
VOUT	Output Voltage	0-VDD	V
TSTG	Storage Temperature	-20 – +60	°C
TOPR	Operating Temperature	0 – +60	°C

Dc Recommended Operating Conditions (Ta=0 – +60°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Power Supply Voltage	4.75	5.0	5.5	V
VIH1	Input High Voltage (A0-A14, D0-D7)	2.2	–	VDD	V
VIL1	Input Low Voltage (A0-A14, D0-D7)	0	–	0.8	V
VIH2	Input High Voltage (A15-A17,/CE1,CE2,/OE,R/W)	4.0	–	VDD	V
VIL2	Input Low Voltage (A15-A17,/CE1,CE2,/OE,R/W)	0	–	1.0	V

DC Characteristics (Ta=0 – +60°C, VDD=4.75 – 5.5 V)

Symbol	Parameter	Condition	Min.	Max.	Unit
ILI	Input Current	0≦VIN≦VDD (A0-A14)	–10	10	μA
		VIN=0V (A15-A17,/CE1,CE2,/OE,R/W)	–1	1	μA
		VIN=VDD (A15-A17,/CE1,CE2,/OE,R/W)	40	60	μA
ILO	Output Leakage Current	/CE1=VIH or CE2=VIL or /OE=VIH	–10	+10	μA
IOH	Output High Current	VOH=2.4V	–1	–	mA
IOL	Output Low Current	VOL=0.4V	2	–	mA
IDDO	Operating Current	/CE1=VIL and CE2=VIH tRC=200nS	–	70	
		32 KByte (CE2,A15-A17=0V or Open)	–	25	mA
IDDS1	VDD Standby Current	64 KByte (/CE1,/OE,R/W)=0V or Open)	–	50μA	
		128 KByte A0-A14=0V-VDD,BCHK=Open D0-D7=0V-VDD	–	100	μA
		32 KByte CE2=0V or Open (Ta=25°C)	–	1.4	μA
		64 KByte VDD=0-3V, All Inputs	–	2.8	μA
		128 KByte and Outputs =0V-VDD	–	5.6	μA
	Battery Leakage	BCHK=Open			
IDDS2	Current at Standby	32 KByte	–	1.4	μA
		64 KByte All pins are open.	–	2.8	μA
		128 KByte (Ta=25°C)	–	5.6	μA

AC Characteristics (Ta = 0 – 60°C, VDD = 4.75V – 5.5V)

Read Cycle

Symbol	Parameter	Min.	Max.	Unit
tRC	Read Cycle Time	250	–	ns
tACC	Address Access Time	–	250	ns
tCO	/CE1 Access Time	–	250	ns
tOE	/OE Access Time	–	100	ns
tCOE	Chip Enable (/CE1,CE2) to Output in Low-Z	35	–	ns
tOEE	Output Enable to Output in Low-Z	15	–	ns
tOD	Chip Enable (/CE1,CE2) to Output in High-Z	–	145	ns
tODO	Output Enable to Output in High-Z	–	85	ns
tOH	Output Data Hold Time	30	–	ns

Write Cycle (R/W Controlled Write)

Symbol	Parameter	Min.	Max.	Unit
tWC	Write Cycle Time	250	–	ns
tWP	Write Pulse Width	90	–	ns
tCW	Chip Selection to End of Write	180	–	ns
tAS	Address Set-up Time	40	–	ns
tWR	Write Recovery Time	20	–	ns
tODW	R/W to Output High-Z	–	90	ns
tOEW	R/W to Output Low-Z	20	–	ns
tDS	Data Set-up Time	40	–	ns
tDH	Data Hold Time	35	–	ns

Write Cycle (/CE1 Controlled Write)

Symbol	Parameter	Min.	Max.	Unit
tWC	Write Cycle Time	250	–	ns
tWP	Write Pulse Width	90	–	ns
tCW	Chip Selection to End of Write	150	–	ns
tAS	Address Set-up Time	40	–	ns
tWR	Write Recovery Time	85	–	ns
tDS	Data Set-up Time	25	–	ns
tDH	Data Hold Time	15	–	ns

AC Test Conditions

Output Load	: 30pF + 1TTL Gate
Input Pulse Level	: 0.4V/3.0V (A0-A14,D0-D7)
	: 0.4V/VDD-0.5V (A15-A17,/CE1,CE2,/OE,R/W)
Timing Measurement (Input)	: 0.8V/2.2V
Timing Measurement (Output)	: 1.5V/1.5V

TIMING WAVEFORMS

READ CYCLE

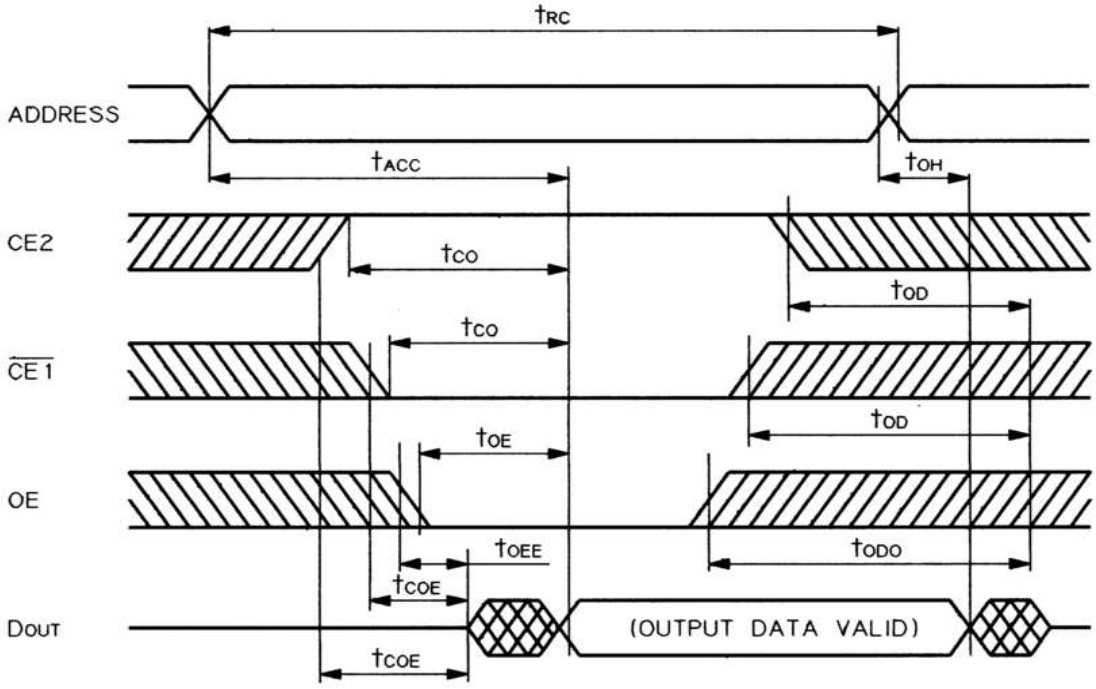


Figure 4-15. Timing Chart

WRITE CYCLE (R/W CONTROLLED WRITE)

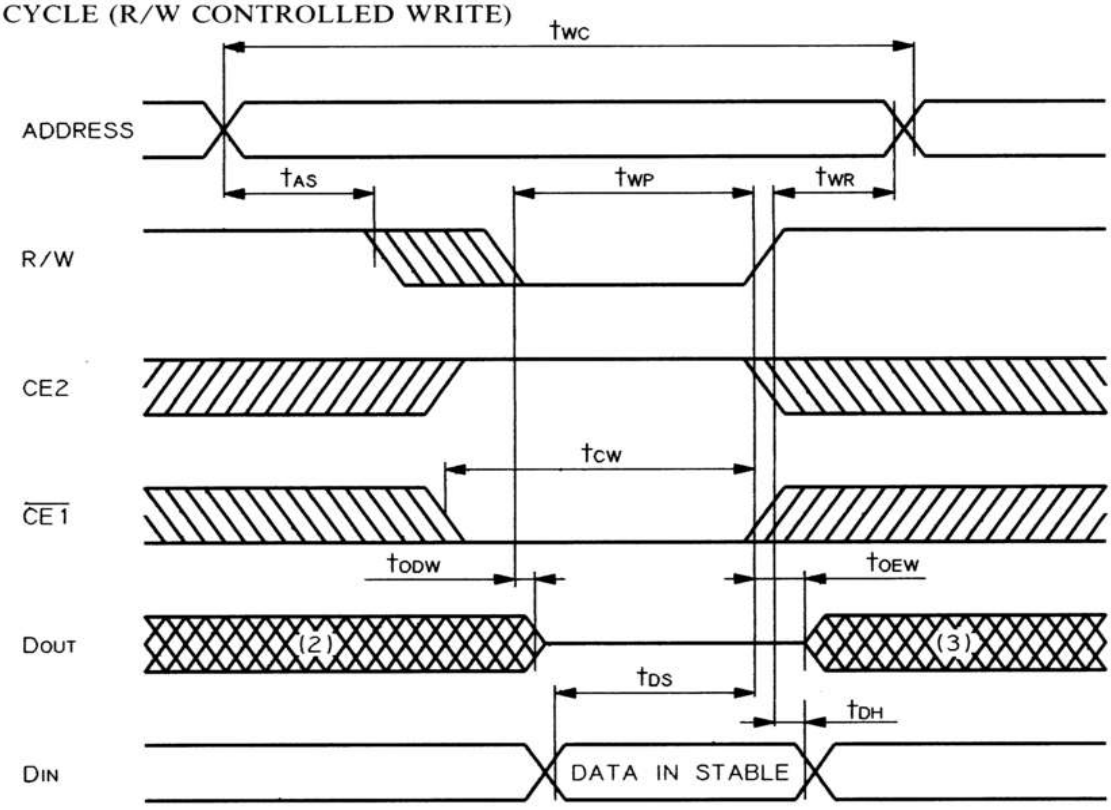


Figure 4-16. Timing Chart

WRITE CYCLE (/CE1 CONTROLLED WRITE)

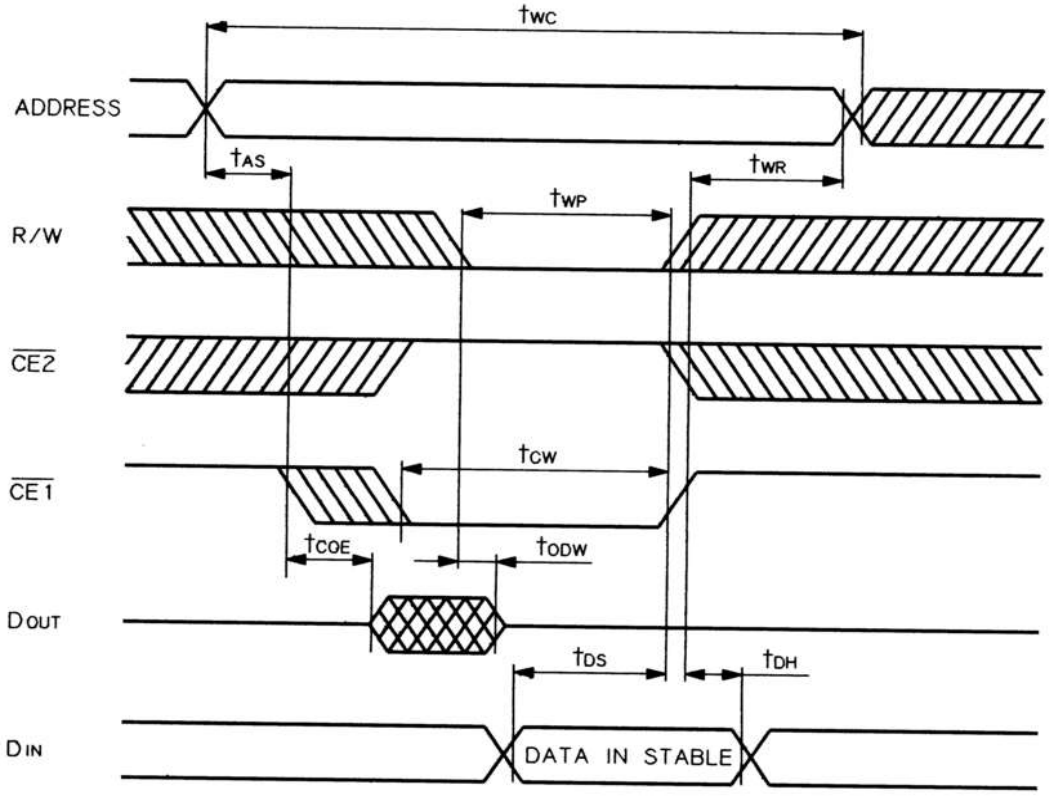


Figure 4-17. Timing Chart

NOTE:

1. R/W is for Read cycle.
2. Assuming that /CE1 Low transition or CE2 High transition occurs coincident with or after R/W Low transition, output remains in a high-impedance state.
3. Assuming that /CE1 High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, output remains in a high-impedance state.
4. Assuming that /OE is high for Write cycle, output is in a high-impedance state during this period.

Data Retention Characteristics (Ta=0°C – 60°C)

Symbol	Parameter	Condition	Min.	Max.	Unit
VDH	Data Retention Supply Voltage		2.3	5.5	V
		32 KByte Ta=25°C	–	1.4	μA
		64 KByte VDD=3V	–	2.8	μA
IDDS2	Battery Leakage Current at Standby	128 KByte (NOTE.1)	–	5.6	μA
		32 KByte Ta=25°C	–	1.4	μA
		64 KByte VDD=3V	–	2.8	μA
		128 KByte (NOTE.2)	–	5.6	μA
tVR	VDD Rising Time		0	20	ms
tVF	VDD Falling Time		0	20	ms
tBSET	Battery Back-up Set-up Time		50	–	ms
tBRCV	Battery Back-up Recovery Time		50	–	ms

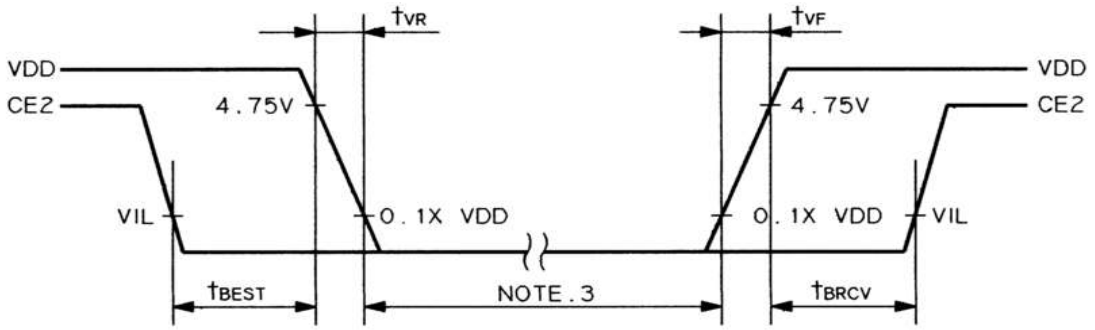


Figure 4-18. Timing Chart

NOTE.1: CE2=0V or Open, VDD=0V – 3V, All Inputs and Outputs =0V-VDD BCHK=Open.
NOTE.2: All pins are open.
NOTE.3: During this period, it is possible to insert or remove a RAM Card.
NOTE.4: RAM Card must be inserted or removed while CE2 is in low or in high impedance.
NOTE.5: RAM Card must not be inserted or removed a while VDD is supplied.

ROM Card

Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Power Supply Voltage	−0.6 – +7.0	V
VIN	Input Voltage	−0.6 – +7.0	V
VI/O	Input/Output Voltage	−0.6 – +7.0	V
TSTG	Storage Temperature	−20 – 60	°C
TOPR	Operating Temperature	0 – 60	°C

Operating Mode

Pin Name	/CE1	/OE	VDD	D0-D7	Power
Mode Read	L	L	5V	Data Out	IDDO
Output Deselect	L	H	5V	Hi-Z	IDDO
Standby	H	*	5V	Hi-Z	IDDS

Read Operation
DC Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	Input High Voltage	2.2	–	VDD+1.0	V
VIL	Input Low Voltage	−0.3	–	0.8	V
VCC	VCC Power Supply Voltage	4.75	5.0	5.25	V

DC Characteristics

Symbol	Parameter					
ILI	Input Current	VIN=0-VDD	–	–	±10	μA
IDDO	Operating Current	/CE1=0V f=5MHz	–	–	40	mA
		Iout=0mA f=1MHz	–	–	10	mA
IDDS	Standby Current	/CE1=VIH	–	–	1	mA
		/CE1=VDD-0.2V	–	–	100	μA
VOH	Output High Voltage	IOH=−400μA	2.4	–	–	V
VOL	Output Low Voltage	IOL=2.1mA	–	–	0.4	V
ILO	Output Leak Current	Vout=0.4V-VCC	–	–	±10	μA

AC Read Characteristics

Symbol	Parameter	Min.	Max.	Unit
tACC	Address Access Time	–	250	ns
tCE	/CE1 Access Time	–	250	ns
tOE	/OE Access Time	–	100	ns
tDF1	/CE1 to Output in High-Z	0	90	ns
tDF2	/OE to Output in High-Z	0	90	ns
tOH	Output Data Hold Time	0	–	ns

AC Test Condition

Output Load	: 1 TTL and 100pF
Input Pulse Rise and Fall Times	: 10ns Max.
Input Pulse Levels	: 0.45V to 2.4V
Timing Measurement Reference Level	: Input 0.8V/2.2V Output 0.8V/2.2V

Capacitance

Symbol	Parameter		Min.	Typ.	Max.	Unit
CIN	Input Capacitance	(VIN=0V)	–	5	10	pF
COUT	Output Capacitance	(VOUT=0V)	–	10	20	pF

This parameter is periodically sampled and not 100% tested.

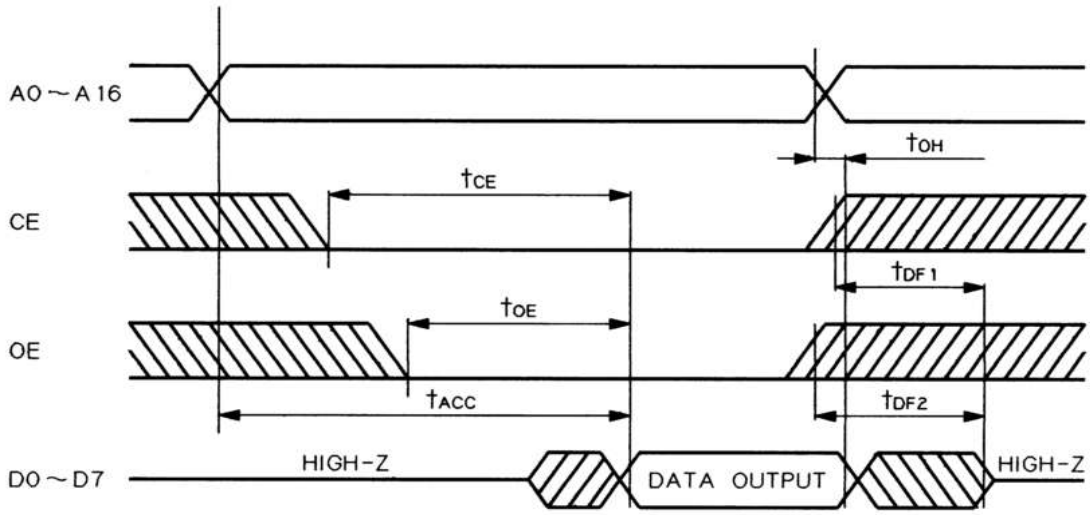
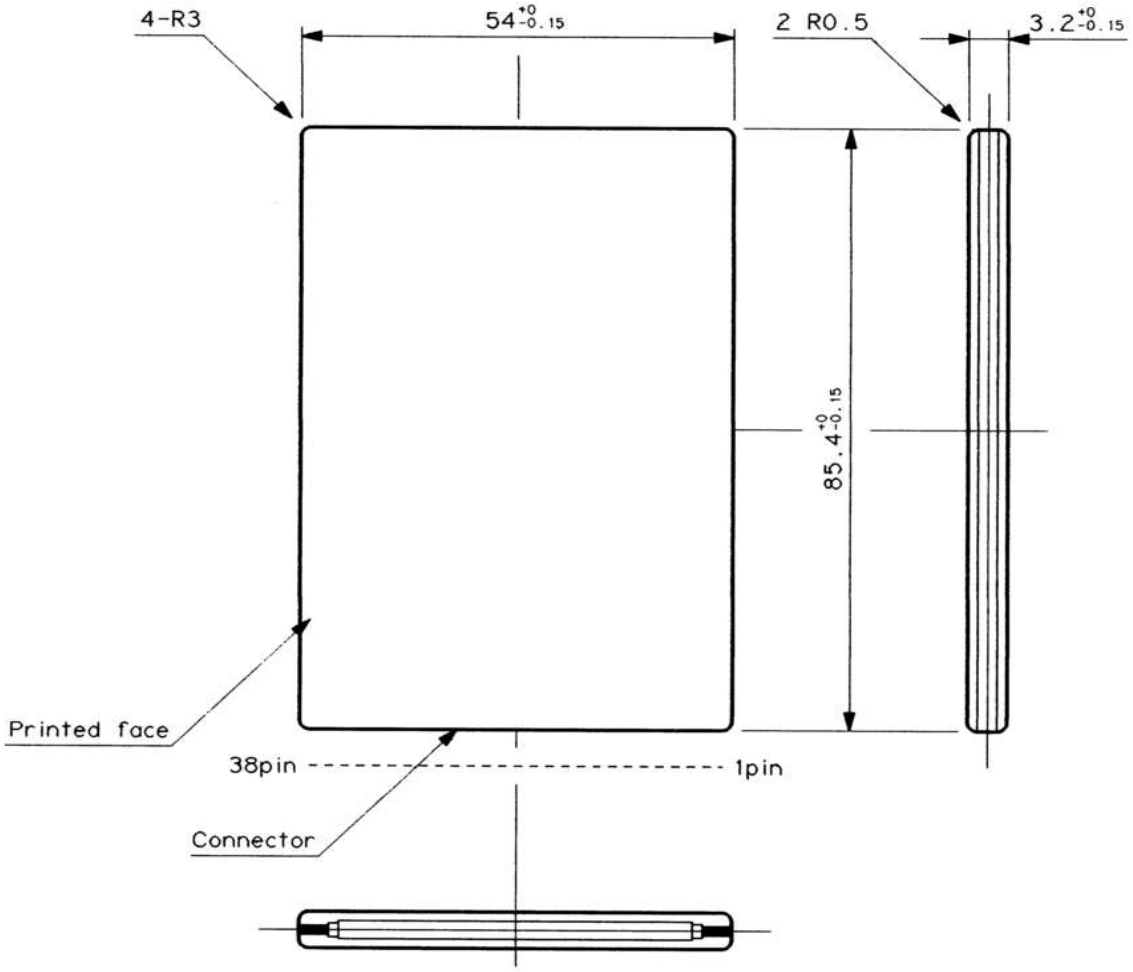


Figure 4-19. Timing Chart

OUTLINE DRAWING
(FRONT SIDE)

UNIT: mm



SPREAD DRAWING OF CONNECTOR SIDE

UNIT: mm

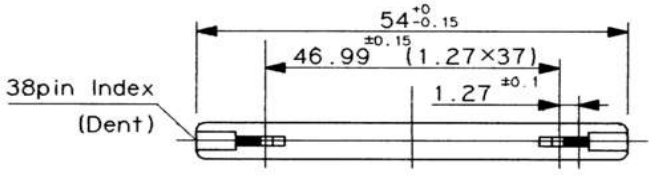
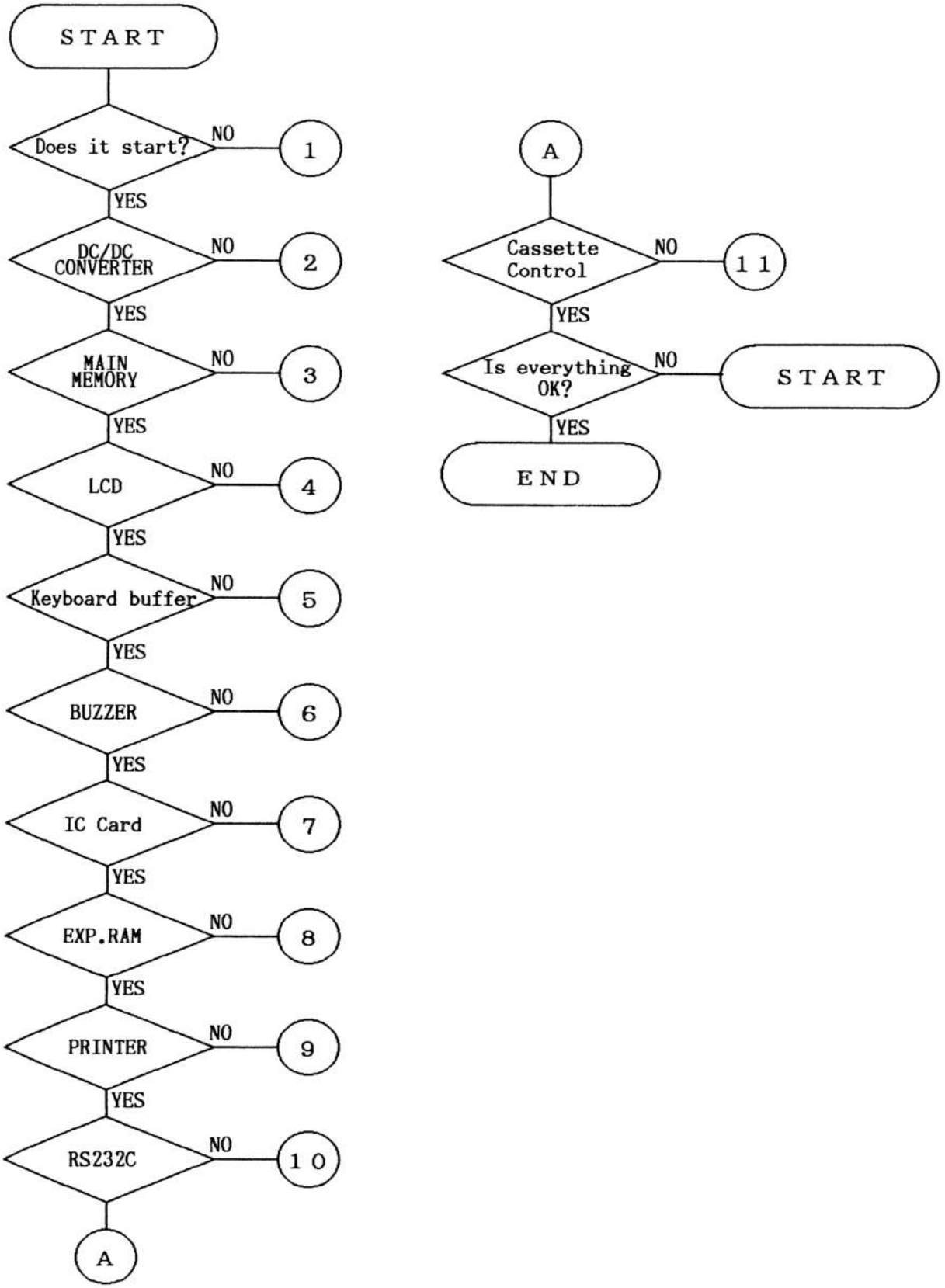
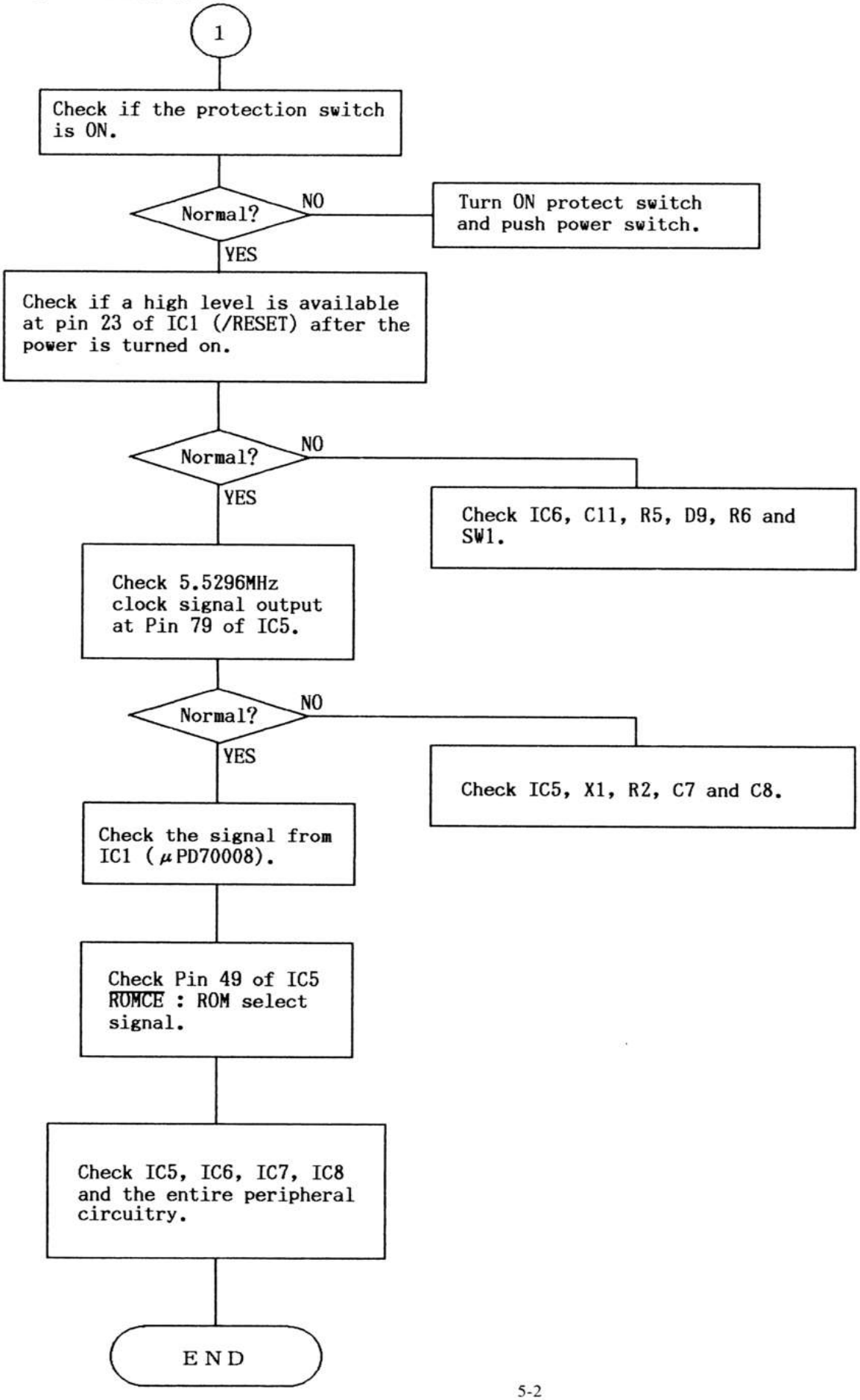


Figure 4-20. IC Card Dimensions

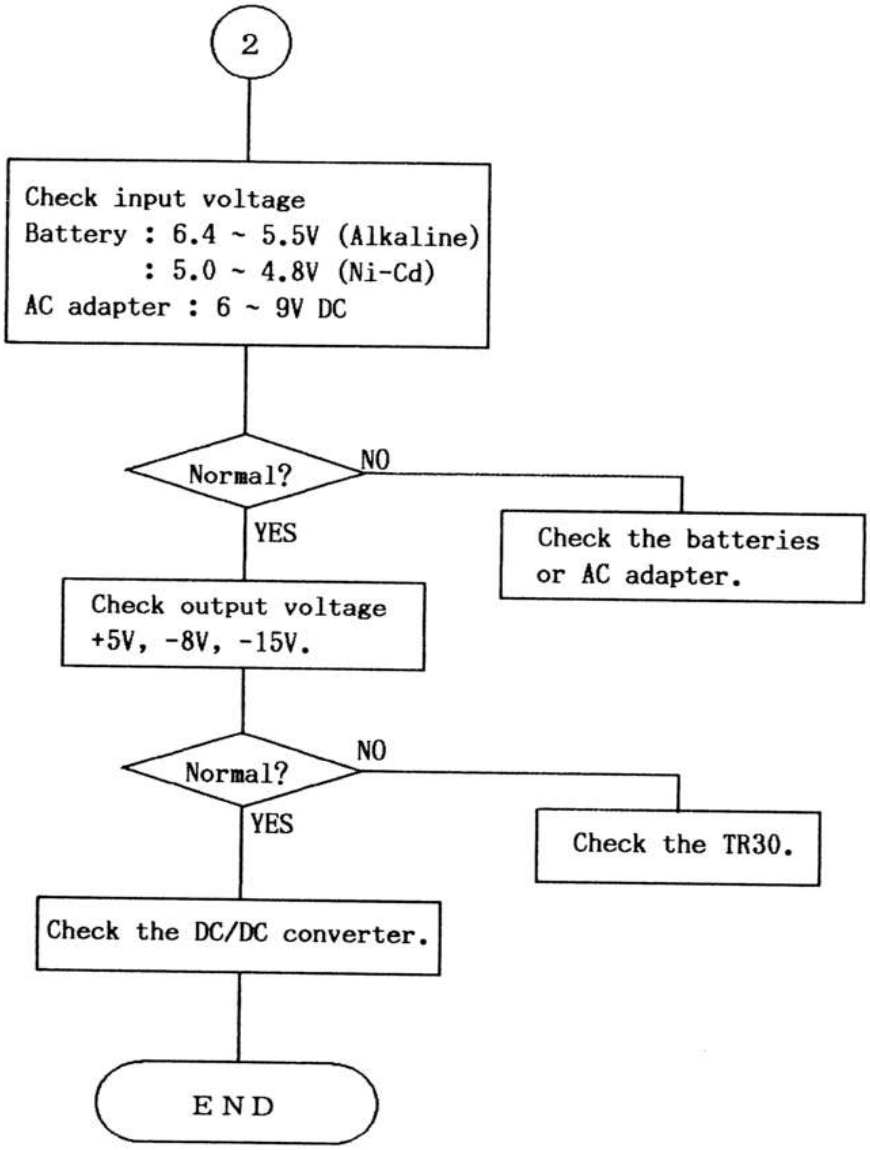
V. TROUBLESHOOTING



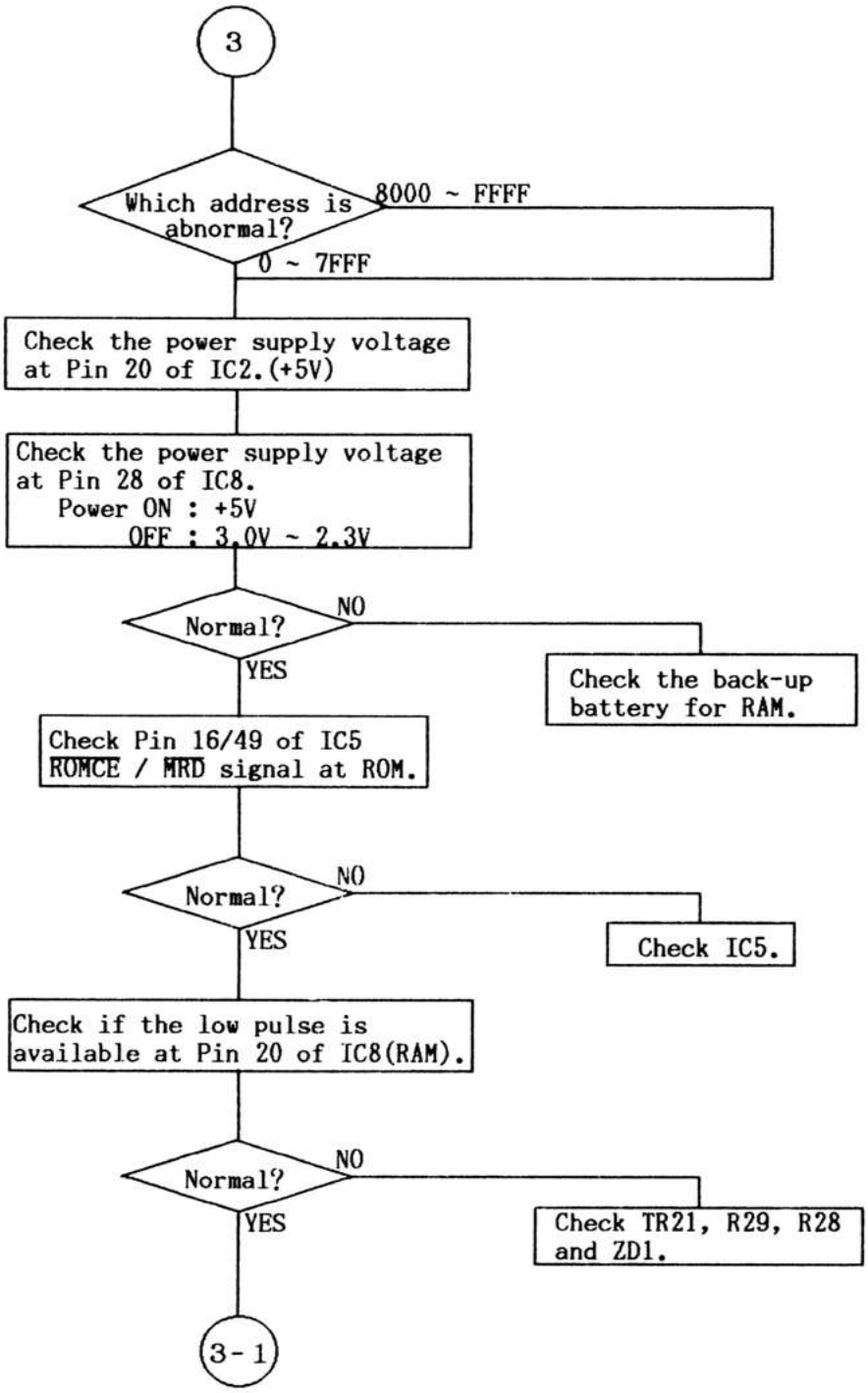
V-1. Will not start

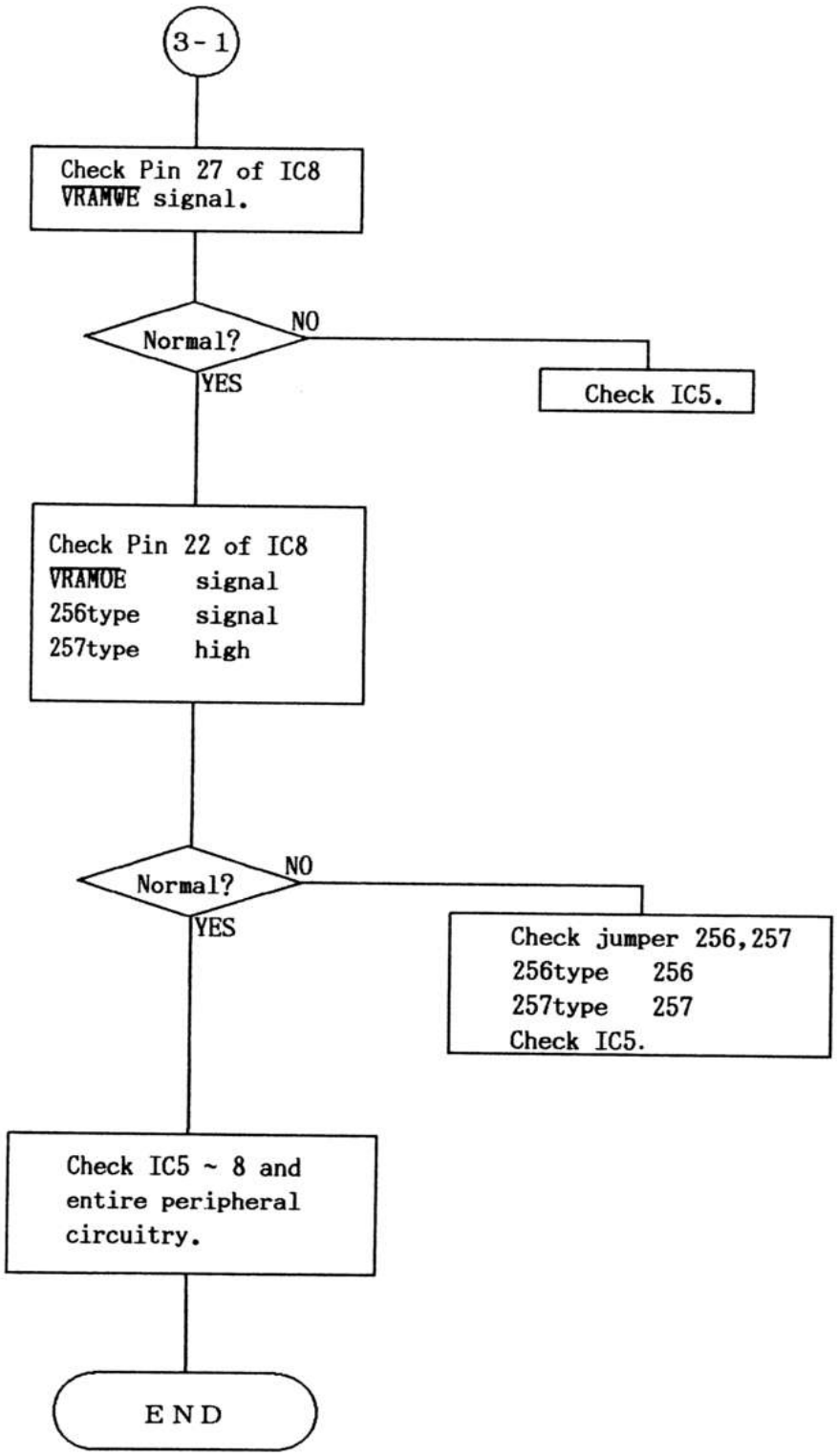


V-II DC/DC Converter Check

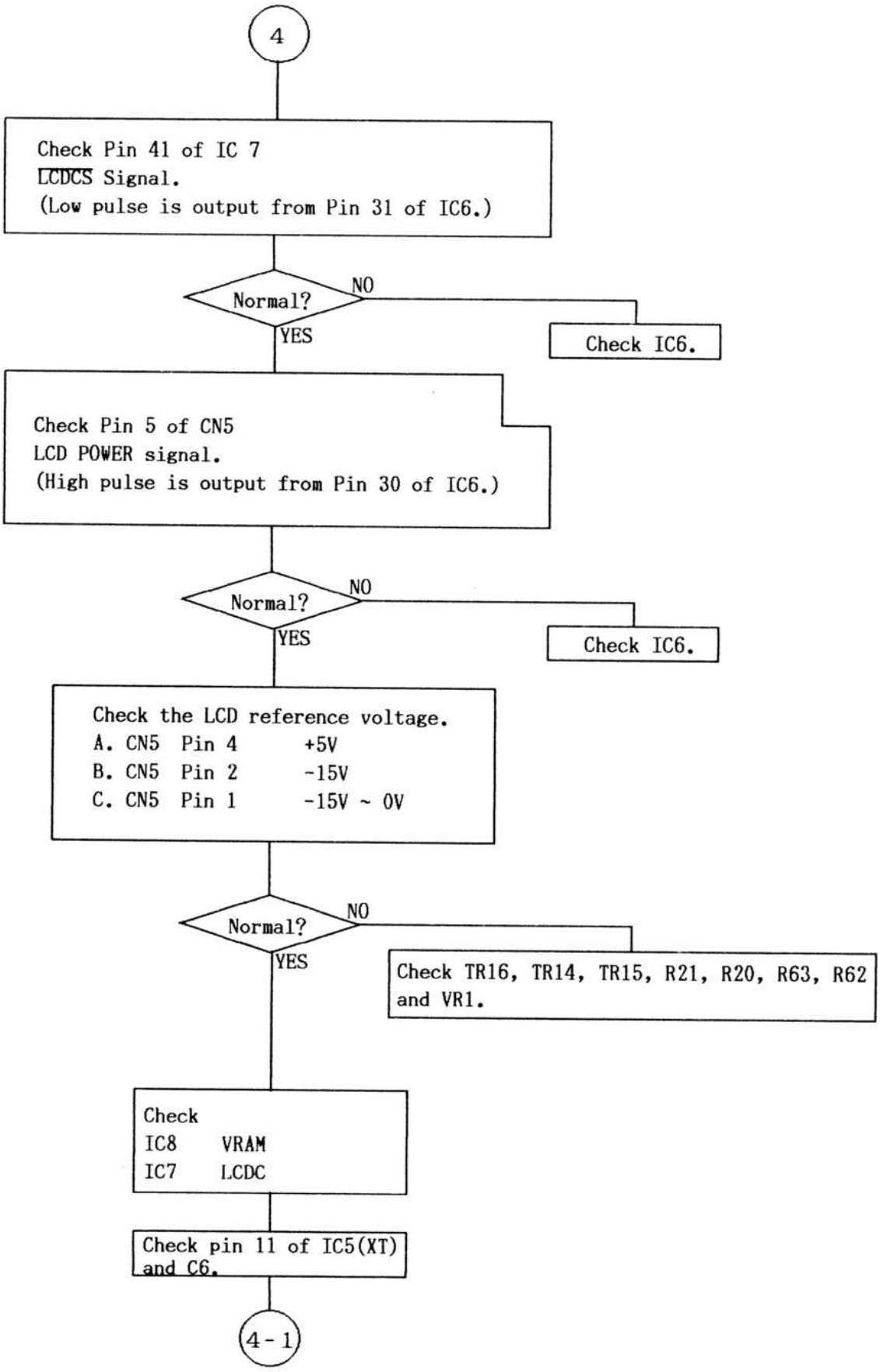


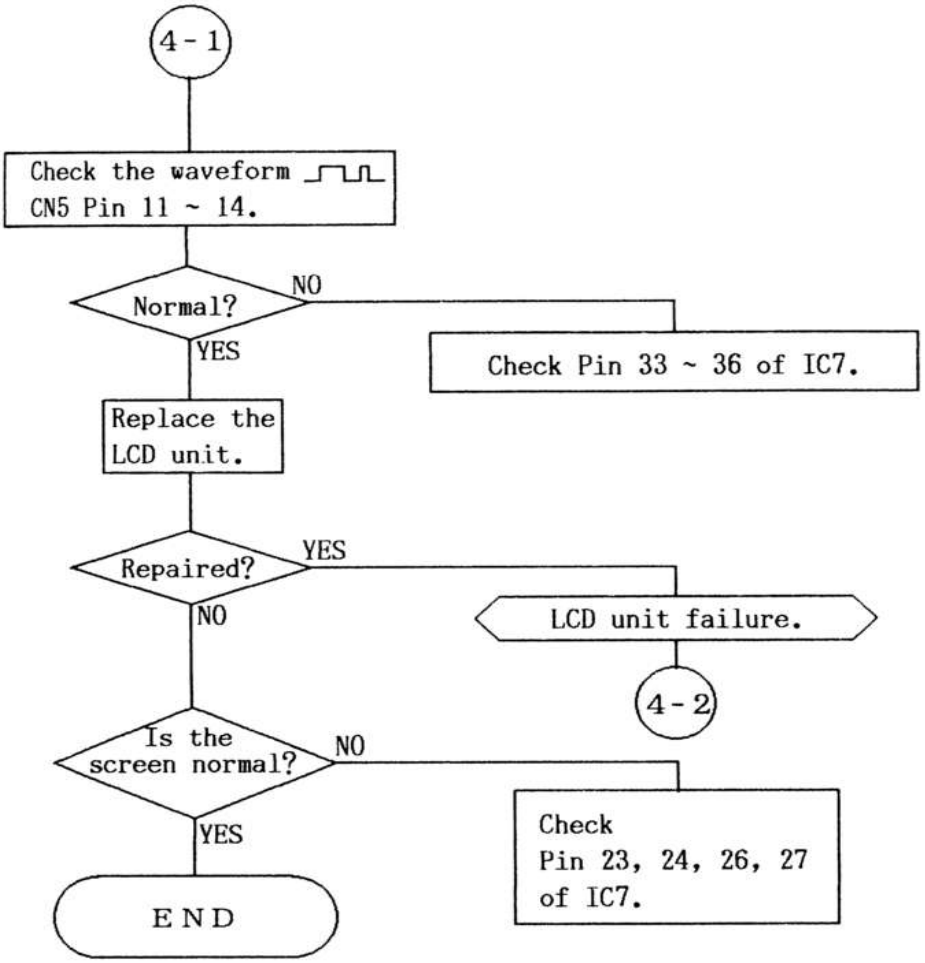
MEMORY Check



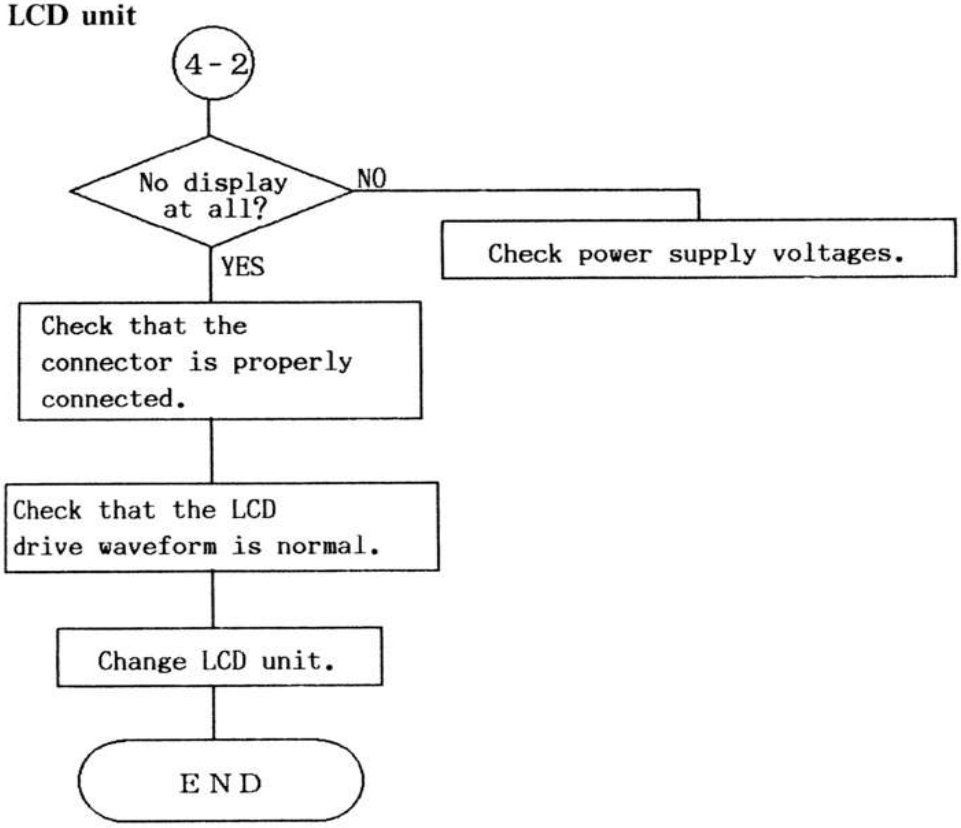

3-1
Check Pin 27 of IC8
VRAMWE signal.
Normal?
NO
YES
Check IC5.
Check Pin 22 of IC8
VRAMOE signal
256type signal
257type high
Normal?
NO
YES
Check jumper 256,257
256type 256
257type 257
Check IC5.
Check IC5 ~ 8 and
entire peripheral
circuitry.
END

LCD

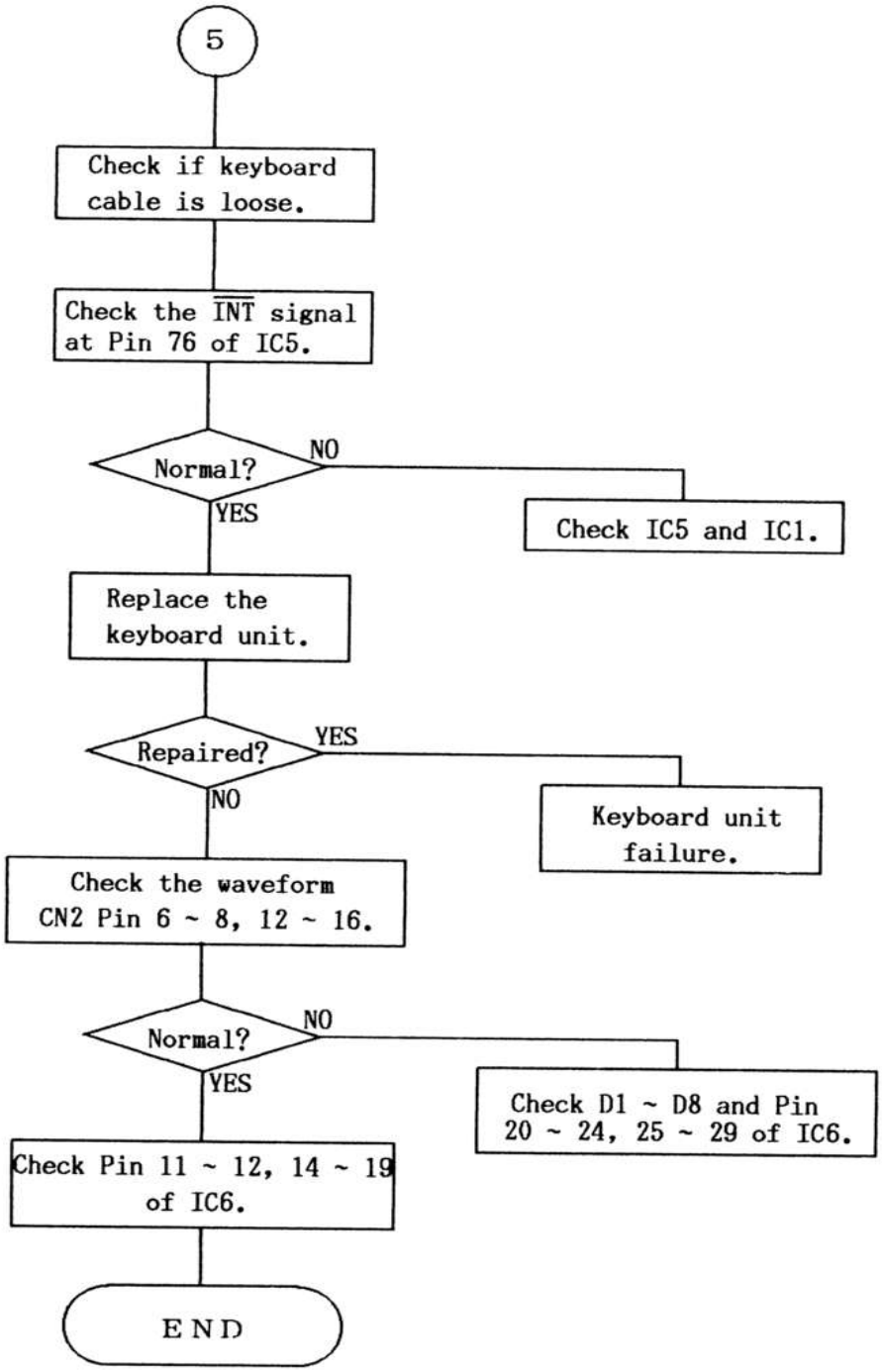

4
Check Pin 41 of IC 7
LCDCS Signal.
(Low pulse is output from Pin 31 of IC6.)
Normal?
NO
YES
Check IC6.
Check Pin 5 of CN5
LCD POWER signal.
(High pulse is output from Pin 30 of IC6.)
Normal?
NO
YES
Check IC6.
Check the LCD reference voltage.
A. CN5 Pin 4 +5V
B. CN5 Pin 2 -15V
C. CN5 Pin 1 -15V ~ 0V
Normal?
NO
YES
Check TR16, TR14, TR15, R21, R20, R63, R62
and VR1.
Check
IC8 VRAM
IC7 LCDC
Check pin 11 of IC5(XT)
and C6.
4 - 1


4 - 1
Check the waveform
CN5 Pin 11 ~ 14.
Normal?
NO
YES
Check Pin 33 ~ 36 of IC7.
Replace the
LCD unit.
Repaired?
YES
NO
LCD unit failure.
4 - 2
Is the
screen normal?
NO
YES
Check
Pin 23, 24, 26, 27
of IC7.
END

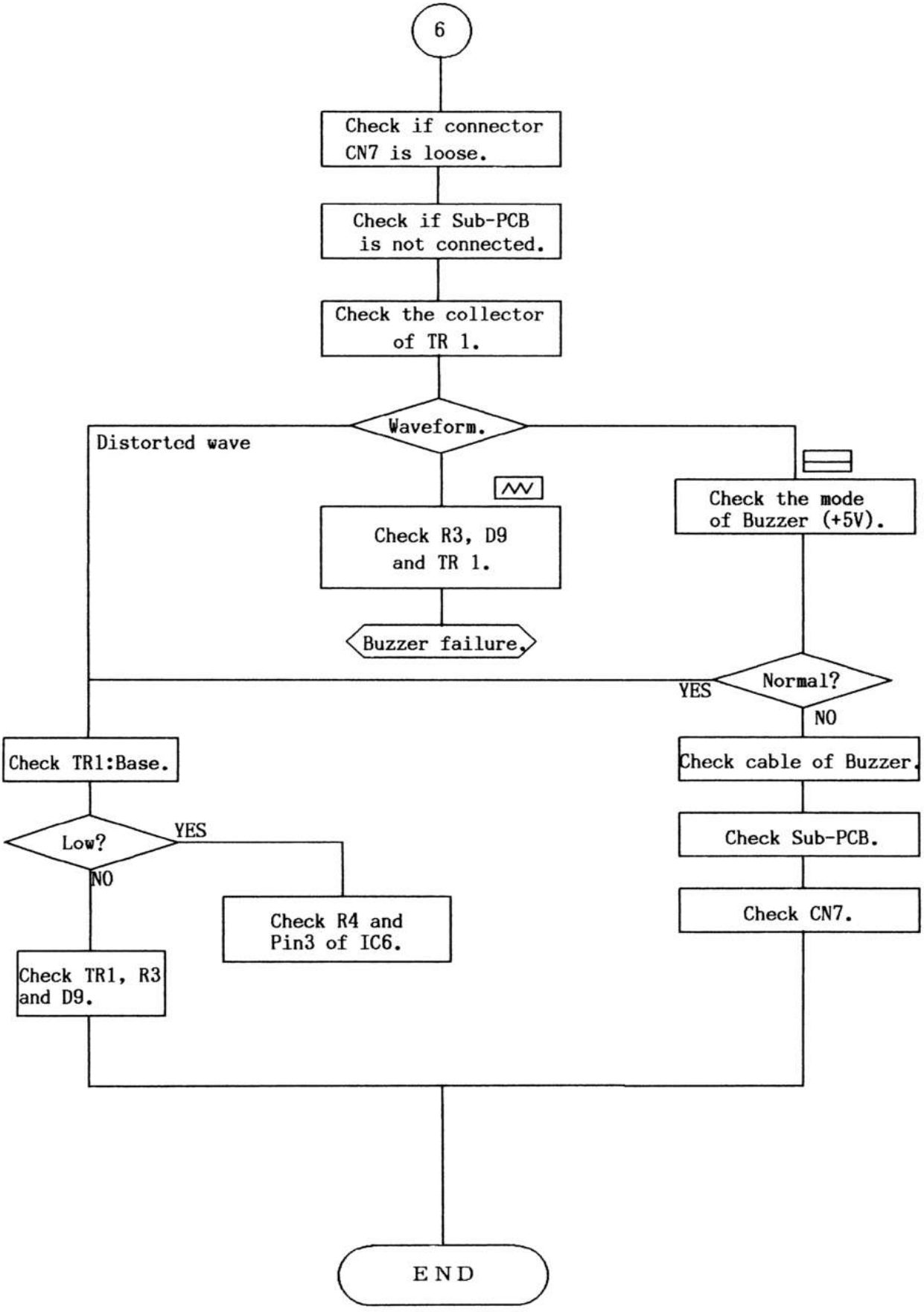
LCD unit


4 - 2
No display
at all?
NO
YES
Check power supply voltages.
Check that the
connector is properly
connected.
Check that the LCD
drive waveform is normal.
Change LCD unit.
END

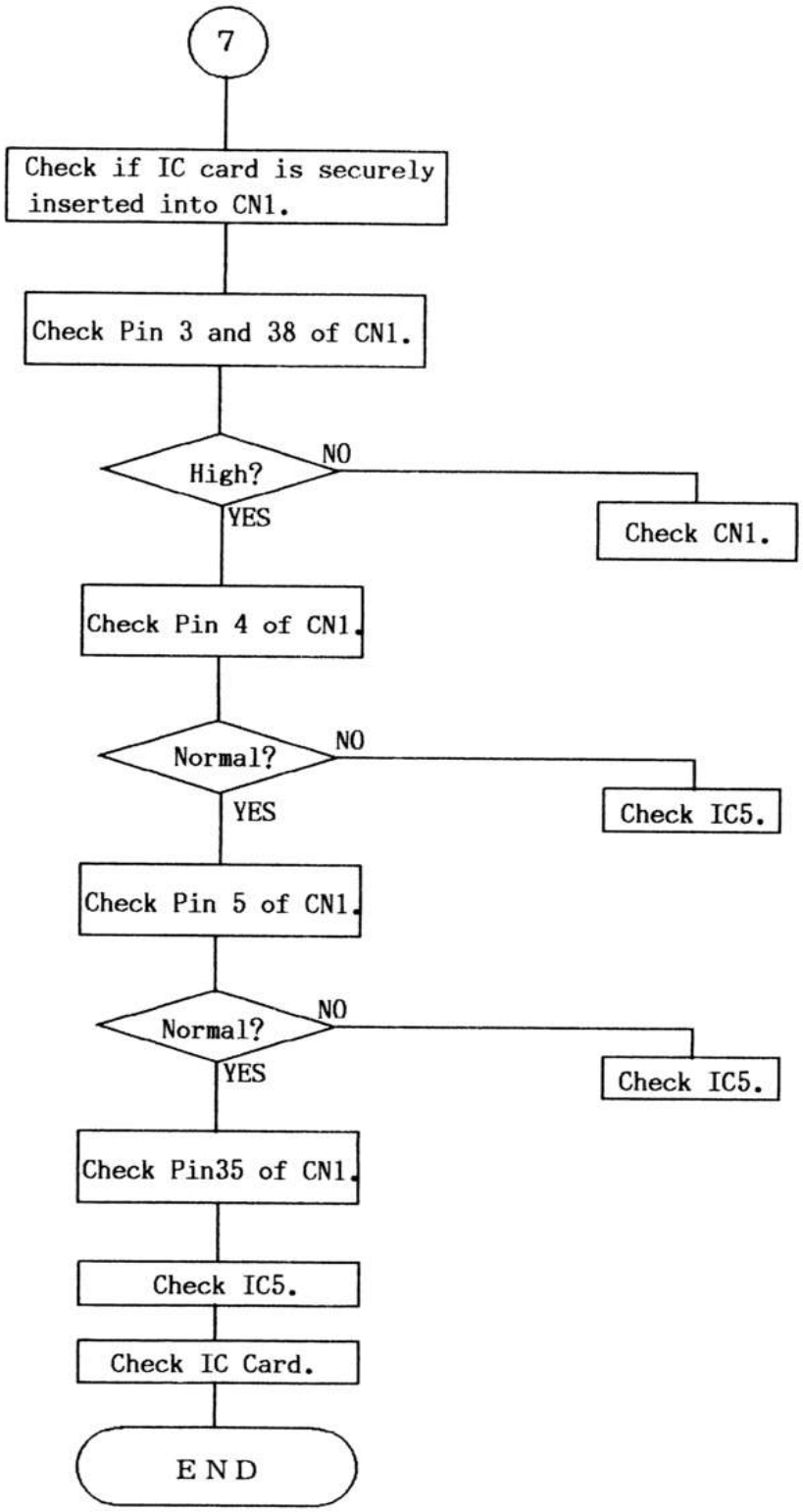
Keyboard buffer



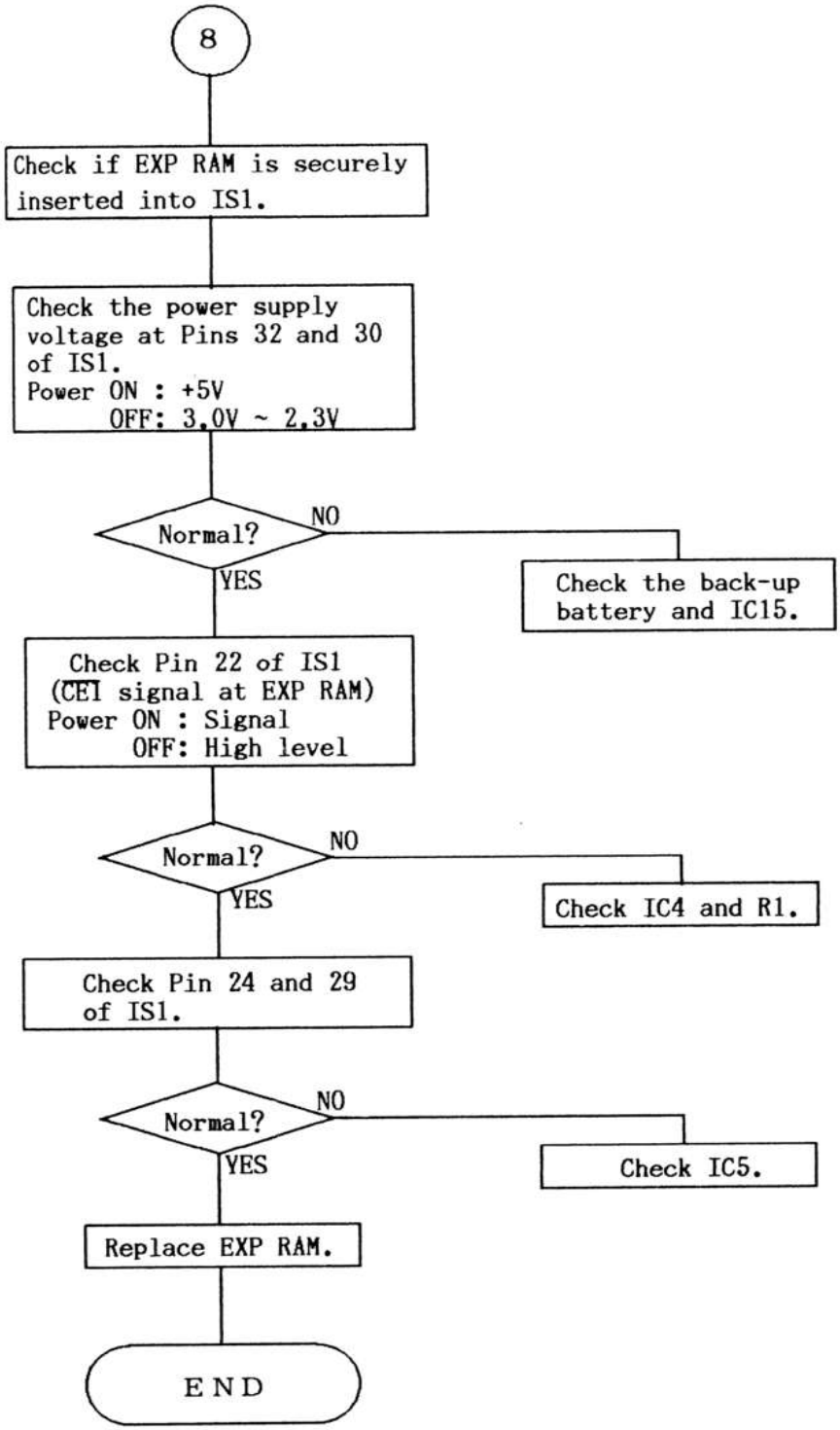
BUZZER check



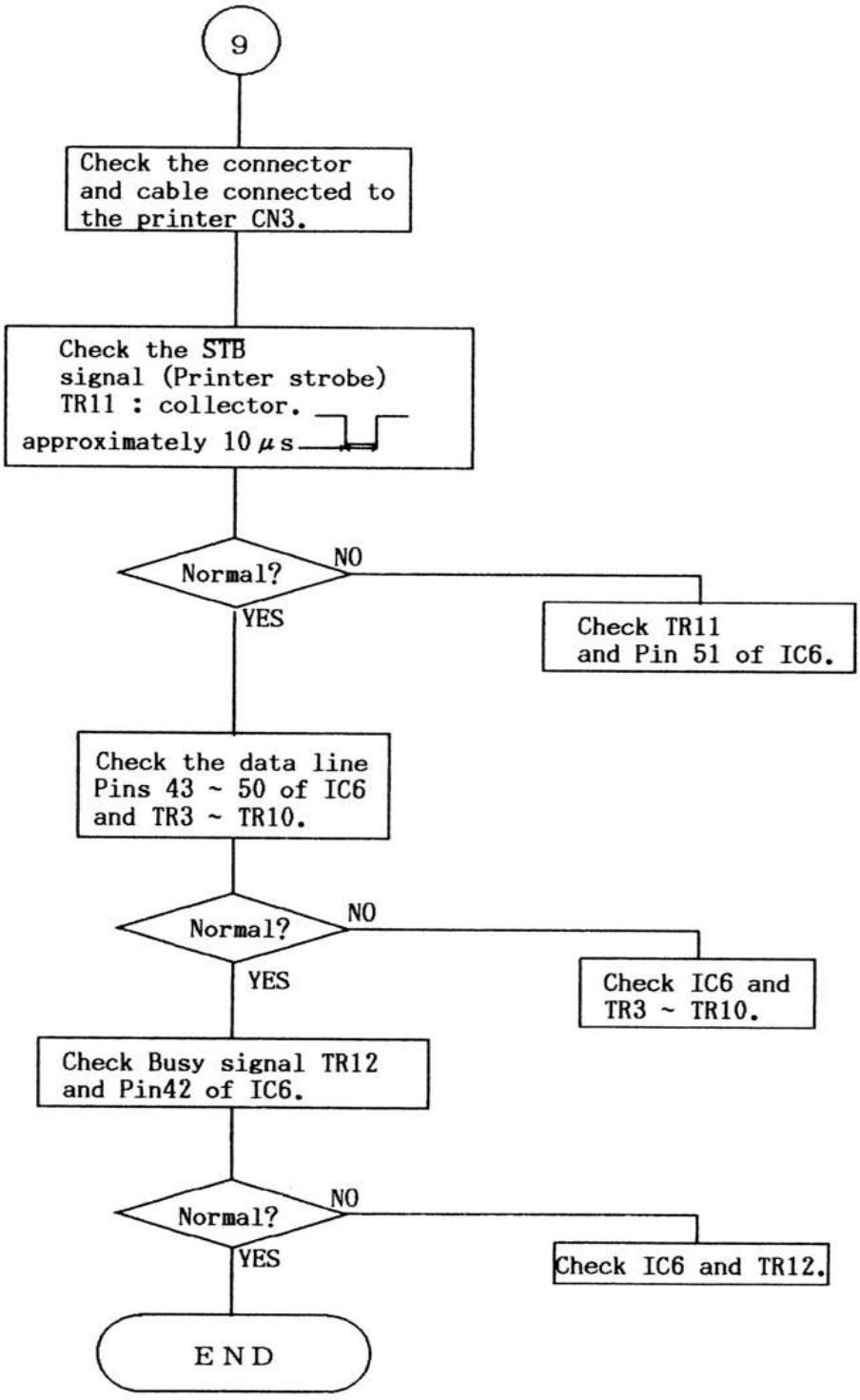
IC Card

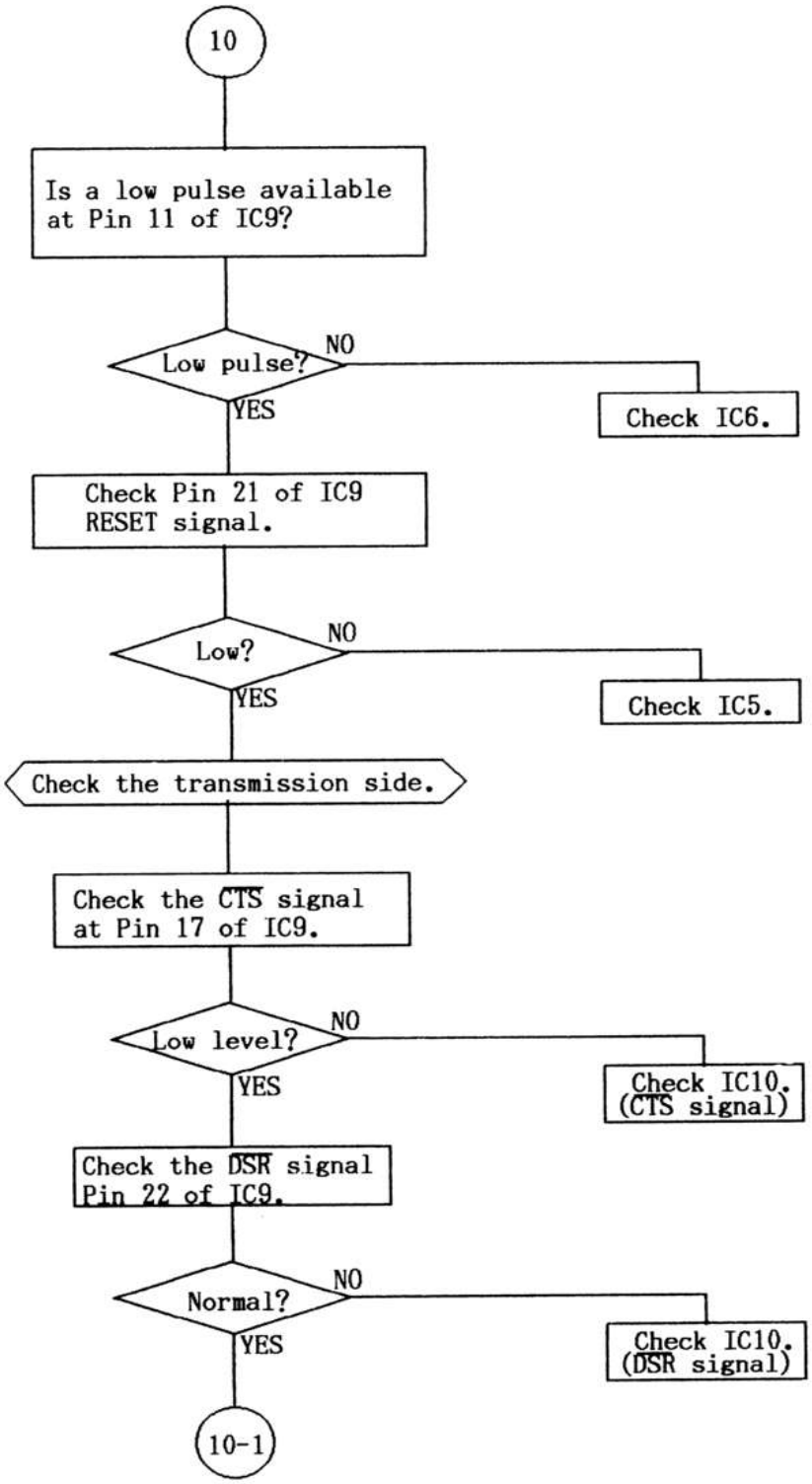

7
Check if IC card is securely inserted into CN1.
Check Pin 3 and 38 of CN1.
High?
NO
YES
Check CN1.
Check Pin 4 of CN1.
Normal?
NO
YES
Check IC5.
Check Pin 5 of CN1.
Normal?
NO
YES
Check IC5.
Check Pin35 of CN1.
Check IC5.
Check IC Card.
END

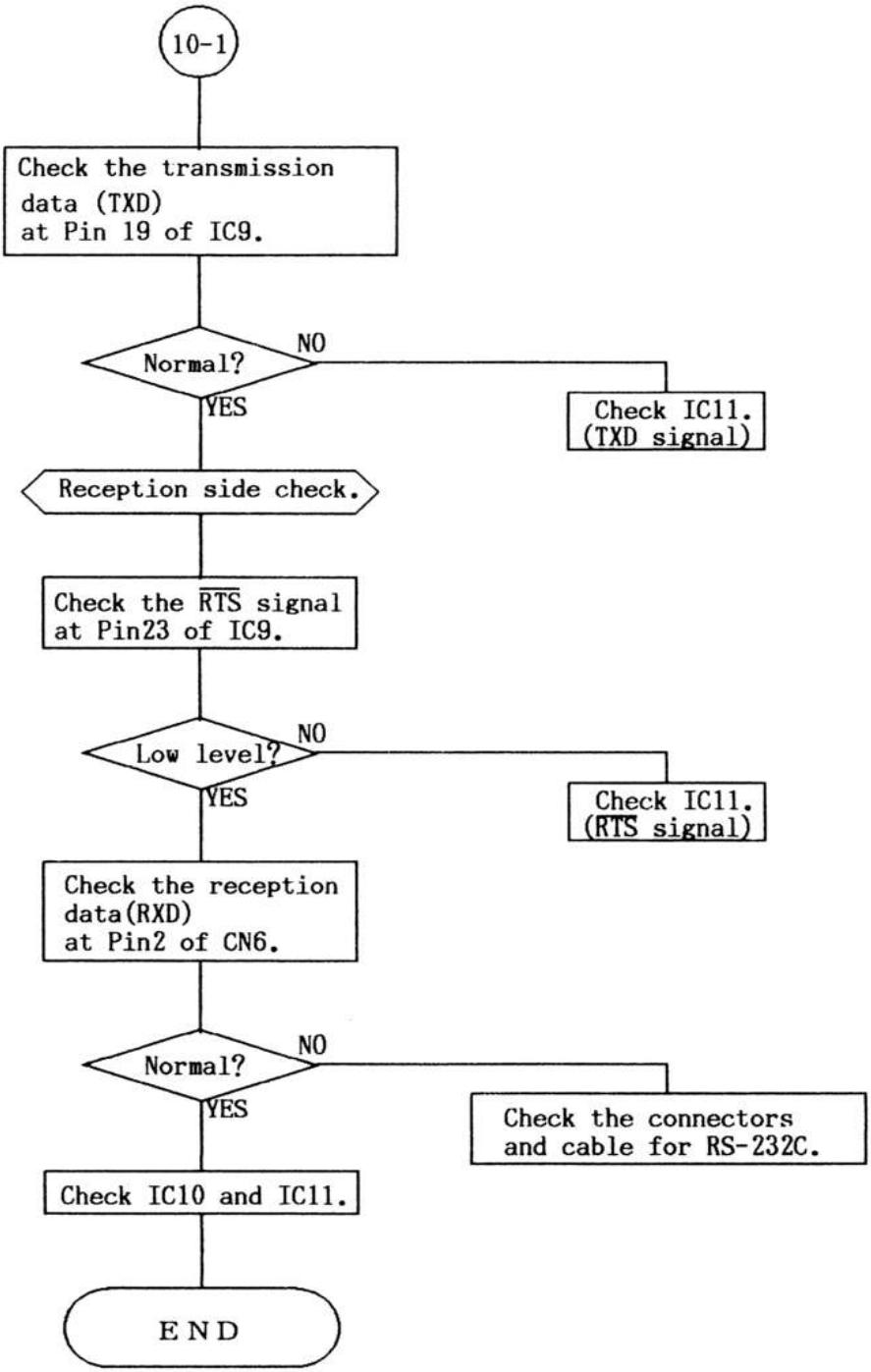
Expansion RAM



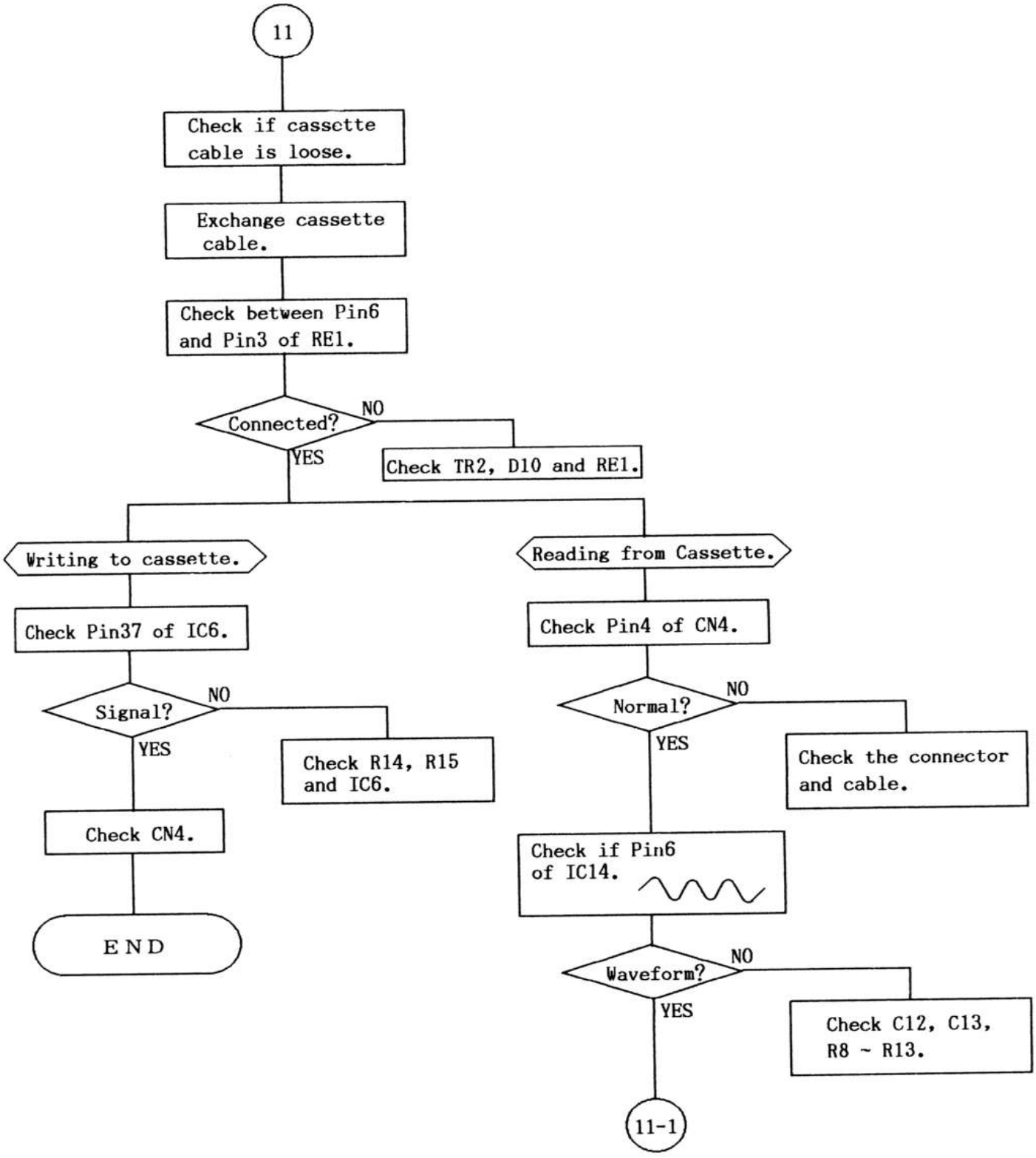
Printer

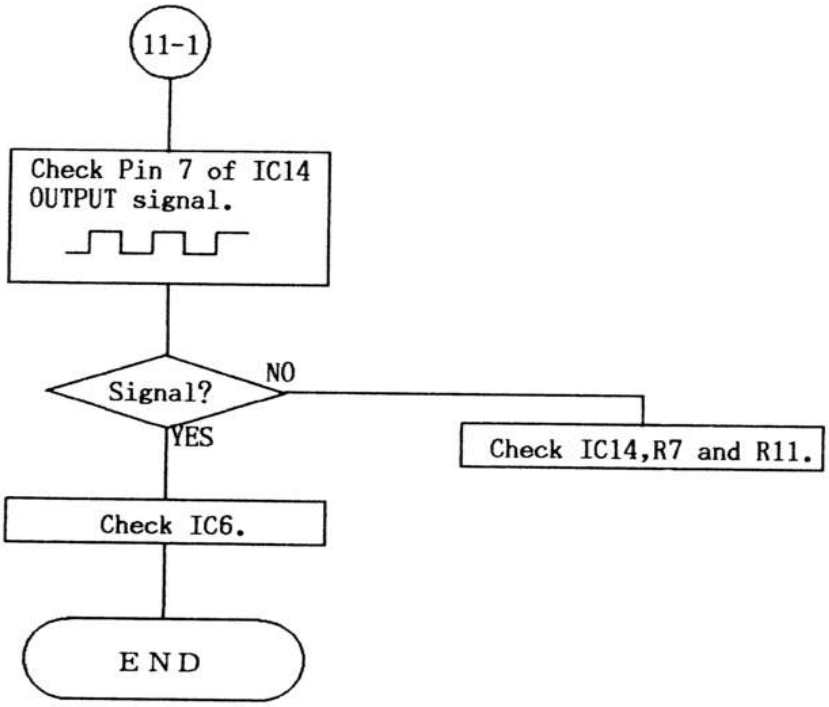

9
Check the connector and cable connected to the printer CN3.
Check the STB signal (Printer strobe) TR11 : collector.
approximately 10 μs
Normal?
NO
YES
Check TR11 and Pin 51 of IC6.
Check the data line Pins 43 ~ 50 of IC6 and TR3 ~ TR10.
Normal?
NO
YES
Check IC6 and TR3 ~ TR10.
Check Busy signal TR12 and Pin42 of IC6.
Normal?
NO
YES
Check IC6 and TR12.
END


10
Is a low pulse available at Pin 11 of IC9?
Low pulse?
NO
YES
Check IC6.
Check Pin 21 of IC9 RESET signal.
Low?
NO
YES
Check IC5.
Check the transmission side.
Check the CTS signal at Pin 17 of IC9.
Low level?
NO
YES
Check IC10. (CTS signal)
Check the DSR signal Pin 22 of IC9.
Normal?
NO
YES
Check IC10. (DSR signal)
10-1


10-1
Check the transmission data (TXD) at Pin 19 of IC9.
Normal?
NO
YES
Check IC11. (TXD signal)
Reception side check.
Check the RTS signal at Pin23 of IC9.
Low level?
NO
YES
Check IC11. (RTS signal)
Check the reception data(RXD) at Pin2 of CN6.
Normal?
NO
YES
Check the connectors and cable for RS-232C.
Check IC10 and IC11.
END

Cassette Control




11-1
Check Pin 7 of IC14
OUTPUT signal.
Signal?
NO
YES
Check IC14,R7 and R11.
Check IC6.
END

VI. EXPLODED VIEW/PARTS LIST

VI-1. Exploded View

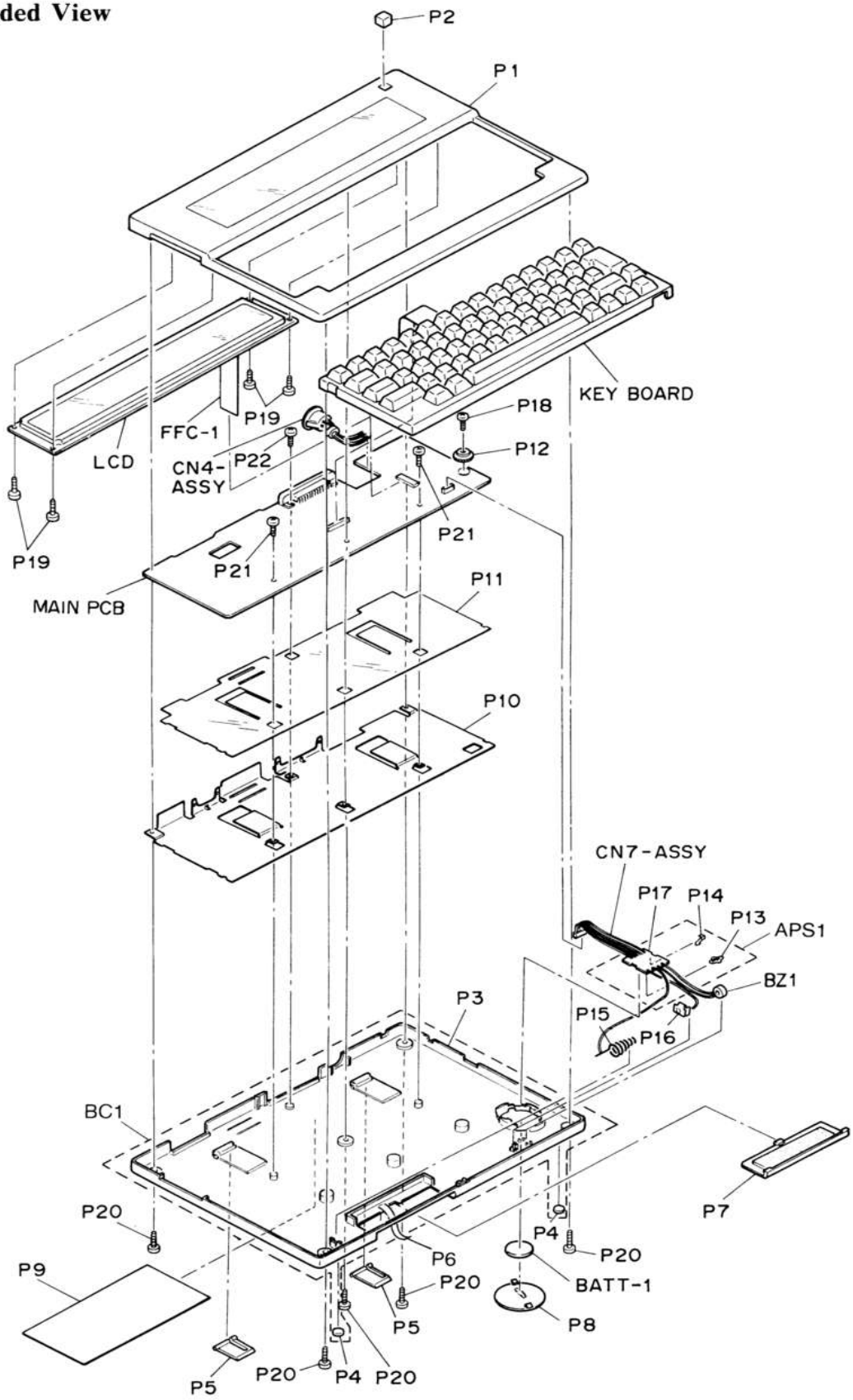


Figure 6-1. Exploded View

VI-2. Electrical Parts List

Main PCB Assembly

REF.NO.	DESCRIPTION	RS PART NO.	MFR's PART NO.
PCB, Main	Assy, PCB, Main		30002030
Beads			
BD1-2	BLM41A04 Ferrite Bead Chip		61500160
Capacitors			
C1-3	Ceramic Chip, 0.1μF 50/25V, +80, −20%		50300520
C4-5	Ceramic Chip, 0.01μF 50/25V, ±10%		50300560
C6	Ceramic Chip, 0.1μF 50/25V, +80, −20%		50300520
C7-8	Ceramic Chip, 33pF 50V, ±5%		50300530
C9-10	Ceramic Chip, 0.1μF 50/25V, +80, −20%		50300520
C11	Electrolytic, 1μF 50V, ±20%		5000140
C12	Ceramic Chip, 0.1μF 50/25V, +80, −20%		50300520
C13	Ceramic Chip, 470pF 25V, ±5%		50300540
C14-16	Ceramic Chip, 0.1μF 50/25V, +80, −20%		50300520
C17-19	Ceramic Chip, 0.01μF 50/25V, ±10%		50300560
C20	Ceramic Chip, 0.1μF 50/25V, +80, −20%		50300520
C21	Ceramic Chip, 0.01μF 50/25V, ±10%		50300560
C22	Ceramic Chip, 0.1μF 50/25V, +80, −20%		50300520
C23	Ceramic Chip, 0.01μF 50/25V, ±10%		50300560
C24	Electrolytic, 10μF 16V, ±20%		50001050
C25	Ceramic Chip, 0.1μF 50/25V, +80, −20%		50300520
C26	Ceramic Chip, 0.01μF 50/25V, ±10%		50300560
C27	Electrolytic, 1μF 50V, ±20%		50001040
C28	Electrolytic, 330μF 16V, ±20%		50001060
C29-30	Ceramic Chip, 470pF 25V, ±5%		50300540
C31	Ceramic Chip, 2200pF 25V, ±10%		50300550
C32	Film, 4700pF, 50V, ±5%		50200100
C33	Electrolytic, 330μF 10V, ±20%		50001400
C34	Electrolytic, 22μF 25V, ±20%		50001080
C35	Electrolytic, 47μF 25V, ±20%		50001090
C36	Electrolytic, 22μF 25V, ±20%		50001080
C37-38	Electrolytic, 10μF 25V, ±20%		50001100
C39-43	Ceramic Chip, 22pF 50V, +20%		50300580
Connectors			
CN1	Male, IC Card connector, 38pin		30501300
CN2	Female, FPC Connector, 16pin		30501310
CN3	Female, PRINTER DB-25pin		30501350
CN5	Female, FPC Connector, 14pin		30501320
CN6	Male, RS-232C DB-9		30501340
CN7	Male, SUB-PCB, 5pin		30501330
Diodes			
D1-8	RLS-73, Silicon		40400210
D9	DAN202K, Silicon		40400220
D10	RLS-73, Silicon		40400210
D11	DAN202K, Silicon		40400220
D12	RLS-73, Silicon		40400210
D13	RB400D, Schottky		40400240
D14-15	RLS-73, Silicon		40400210
D16	RB110C, Schottky		40400250
D17	RLS-92, Silicon		40400230

REF.NO.	DESCRIPTION	RS PART NO.	MFR's PART NO.
D18	RB110C, Silicon		40400250
D19-20	RLS-92, Silicon		40400230
D21	RLS-73, Silicon		40400210
Filters			
F1-2	TH3820B, Four-Terminal Filter Type, Filmac		61500180
Ferrite Core			
FC1	2643-002402, Ferrite Core		61500190
Integrated Circuits			
IC1	D70008A-6, 6MHz, CPU, CMOS		40000820
IC2	D23C2000G, 2Mbit, MASK ROM, CMOS		42100060
IC4	C9(TC4S66F), CMOS		42000010
IC5	M60014-0142FP, Gate Array, CMOS		40000840
IC6	M60011-0152FP, Gate Array, CMOS		40000850
IC7	M6255, LCD Controller, CMOS		40000750
IC8	D43257GU-10L/12L M5M5256FP-10L/12L HM62256LFP-8T/10T/125 SRM20256LM-12, SRAM, COMS		42100070
IC9	D71051GU, Serial Controller		40000870
IC10	DS14C89AM, RS232C Receiver, CMOS		42000020
IC11	DS14C88M, RS232C Driver, CMOS		42000030
IC12	HC14, HEX Schmitt-Trigger Inverter, CMOS		40300410
IC13	HC74, D-Flip-Flop, CMOS		40300380
IC14	2903, Comparator, Linear-IC		41600060
IC15	T529L, Reset IC		42000040
IC Socket			
IS1	IC Socket, 32pin		31600050
Jack			
JAC1	JACK AC		31000040
Coil Inductors			
L1	CHKL-01, 15μH, 1A		61100080
L2	SP0406-390k-6, 39μH		61100090
L3-4	LQH3C220K03M00-01, 22μH, 250mA, Chip		61100100
Resistors (All resistors are 1/10W, $\pm$5%, Metal Glaze Chip)			
R1	47K ohm		51300920
R2	1M ohm		51300960
R3	10K ohm51300840		
R4	27K ohm		51300880
R5	100K ohm		51300930
R6	200 ohm		51300740
R7	1K ohm		51300790
R8-10	12K ohm		51300850
R11	1M ohm		51300960
R12-13	2.2K ohm		51300820
R14	2K ohm		51300810
R15	220 ohm		51300750
R16-17	100K ohm		51300930
R18-19	10K ohm		51300840
R20	100K ohm		51300930
R21	1K ohm		51300790
R22	200 ohm		51300740

REF.NO.	DESCRIPTION	RS PART NO.	MFR's PART NO.
R23-24	100K ohm		51300930
R25	200 ohm		51300740
R26-27	10K ohm		51300840
R28	510 ohm		51300770
R29	4.7K ohm		51300830
R30	30K ohm		51300890
R32	620 ohm		51300780
R33-34	100K ohm		51300930
R35	620K ohm		51300950
R36	100K ohm		51300930
R37	15K ohm		51300860
R38	100K ohm		51300930
R39	10K ohm		51300840
R40	100K ohm		51300930
R41-42	39K ohm		51300910
R43	10K ohm		51300840
R44	330K ohm		51300940
R45	100K ohm		51300930
R46	10K ohm		51300840
R47	18K ohm		51301050
R48	100K ohm		51300930
R49	47K ohm		51300920
R50-52	10K ohm		51300840
R53-54	4.7K ohm		51300830
R55	1K ohm		51300790
R56	470 ohm		51300760
R57	820K ohm		51301410
R58	15K ohm		51300860
R59	10 ohm		51300730
R60	10K ohm		51300840
R61	1K ohm		51300790
R62	33K ohm		51300970
R63	20K ohm		51300870
R64	1K ohm		51300790
R66-R81	1K ohm		51300790
Resistor Networks:	resistor networks are 1/8W, +5%		
RA1-2	100K ohm × 8		51500570
RA3	10K ohm × 8		51500400
RA4-5	100K ohm × 5		51500610
RA6	10K ohm × 8		51500400
Relay			
RE1	24V DC, 1A		32200020
Switches			
SW1	HKW0614-01-010, Reset Switch		31200570
SW2	KMC-V01AV, Power Switch		31200560
SW3	SSF-022Z, Protect Switch		31200580
Transformer			
T1	CHKT-01, Transformer DC/DC Converter		61200320
Transistors			
TR1	2SC2412K, NPN type		41000230
TR2-13	DTC114EK, NPN type (Degitra)		41000250

REF.NO.	DESCRIPTION	RS PART NO.	MFR's PART NO.
TR14	2SA1037K, PNP type		40800130
TR15	2SC2412K, NPN type		41000230
TR16-18	DTC114EK, NPN type (Degitra)		41000250
TR19	2SA1037K, PNP type		40800130
TR20-22	2SC2412K, NPN type		41000230
TR23	DTA114EK, PNP type (Degitra)		40800140
TR24	2SC2412K, NPN type		41000230
TR25	2SA1037K, PNP type		40800130
TR26	DTC114EK, NPN type (Degitra)		41000250
TR27-28	2SC2412K, NPN type		41000230
TR29	2SA1037K, PNP type		40800130
TR30	2SC3518K-Z, NPN type		41000240
TR31	DTA114EK, PNP type		40800140
Potentiometer			
VR1	100K ohm, 1/10W, ±30%		51400100
Trimmer Resistor			
VR2	5K ohm, 1/10W, Chip		51400110
Wire			
UL1007, TR-64, 1 × 24 AWG GREEN WIRE-GREEN			60400250
Ceramic Resonator			
X1	5.53MHz		62000260
Zener Diodes			
ZD1-3	MZK4B/RLZJ3.9A		40500420
ZD4	MZK7A/RLZ6.8C		40500490

LCD Unit

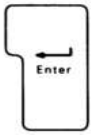
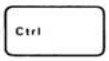
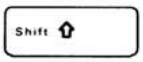
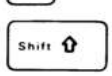
REF.NO.	DESCRIPTION	RS PART NO.	MFR's PART NO.
Capacitors			
LC1-6	Electrolytic,4.7 μF,35V		50001140
LCB	Electrolytic,4.7 μF,35V		50001140
LCb1-5	Not used		
LCP6	Electrolytic,4.7 μF,35V		50001140
Connector			
LCN1	Female, FPC, 14pin		30501420
Integrated Circuits			
LIC1-6	M5299/M5299A, Common Driver		40000970
LIC7	M5298B/M5298A, Segment Driver		40000960
LIC8	2902M/UPC324G/BA10324F/AN1324NS, OP-Amplifier		41600070
LIC9	E5021		42000090
Transistors			
LQ1-2	2SA1235, PNP type		40800180
Resisters			
LR1-2	7.5 Kohm, 1/8W, $\pm$1%, Metal Glaze Chip		51300980
LR3	39 Kohm, 1/8W, $\pm$2%, Metal Glaze Chip		51300990
LR4-5	7.5 Kohm, 1/8W, $\pm$1%, Metal Glaze Chip		51300980
LRh	100 ohm, 1/8W, $\pm$2%, Metal Glaze Chip		51300100

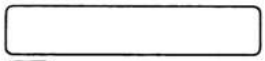
REF.NO.	DESCRIPTION	QTY	RS PART NO.	MFR's PART NO.
P1	Case, Top, Black	1		10000980
P2	Power Key, Blue	1		20404950
BC1	Assembly, Case, Bottom	1		10400420
P3	Case, Bottom, Black	1		
P4	Foot, Rubber, Black	2		
P6	Strap, Removal, Battery	1		
P5	Stand	2		25000070
P7	Cover, Battery, Main, Black	1		11900150
P8	Cover, Battery, Backup, Black	1		11900130
P9	Label International Keyboard List	1		71101130
P10	Shield Plate, PCB, MAIN	1		32600070
P11	Insulator, PCB, MAIN	1		33200020
P12	Knob, Contrast, Black	1		20200210
APS1	Assembly, PCB, SUB	1		30002390
P13	Backup Electrode, Negative	1		
P14	Backup Electrode, Positive	1		
P17	PCB, SUB	1		
P15	Spring Electrode, Negative	1		32300130
P16	Main electrode, Positive	1		32300140
HWK1	Hard Ware kit	1		93000010
P18	Screw, Pan Head, Hard Ware kit, M 1.7 × 3.5	1		90000710
P19	Screw, Tapping Btp 2.6 × 5	4		90000700
P20	Screw, Tapping Btp 2.6 × 12	5		90000400
P21	Screw, Tapping Btp 2.6 × 5	2		91700040
P22	Screw, Tapping Btp 2.6 × 8	1		90000590
BATT-1	Battery, Lithium, CR2430	1		30900240
BZ-1	Buzzer, CB-12H	1		31100140
CN4-ASSY	Connector, Female, Cassettee Din, 8-pin			32300120
CN7-ASSY	Connector, PCB SUB, 5-pin	1		60500540
FFC-1	Cable, Flexible Flat LCD 14-pin	1		60200800
KEYBOARD	Keyboard U.S.A	1		23400030
LCD	Assy, Display, LCD	1		32500040
PCB, MAIN	Assy, PCB, MAIN	1		30002030
S.C-1	Slip Case	1		72800140

Keyboard Unit

REF.NO.	DESCRIPTION	QTY	RS PART NO.	MFR's PART NO.
K1	Frame	1		20100130
K2	Membrane	1		30101820
K3	Metal Plate	1		23600230
K5	Guide Chip/Contact Rubber	62		20500070
K6	Click Rubber for Standard Keytops	61		22500050
K7	Click Rubber for Space Keytops	1		22500060
K8	Spring	2		21900780
K9	Crank Guide for Enter Keytop	2		24600070
K10	Crank Shaft for Enter Keytop	1		22900090
K11	Crank Shaft for Shift Keytop	1		22900100
K12	Crank Shaft for Space Keytop	1		22900110
K13	Tape	2		23700160
K14	Screw	15		90000720

REF.NO.	DESCRIPTION	QTY	RS PART NO.	MFR's PART NO.
KEY TOPS				
K15	Set, Keytops	1		22700270
KPQ-1	Key Top	1		
KPQ-2	Key Top	1		
KPQ-3	Key Top	1		
KPQ-4	Key Top	1		
KPQ-5	Key Top	1		
KPQ-6	Key Top	1		
KPQ-7	Key Top	1		
KPQ-8	Key Top	1		
KPQ-9	Key Top	1		
KPQ-10	Key Top	1		
KPQ-11	Key Top	1		
KPQ-12	Key Top	1		
KPQ-13	Key Top	1		
KPQ-14	Key Top	1		
KPQ-15	Key Top	1		
KPQ-16	Key Top	1		
KPQ-17	Key Top	1		
KPQ-18	Key Top	1		
KPQ-19	Key Top	1		
KPQ-20	Key Top	1		
KPQ-21	Key Top	1		
KPQ-22	Key Top	1		
KPQ-23	Key Top	1		
KPQ-24	Key Top	1		
KPQ-25	Key Top	1		
KPQ-26	Key Top	1		
KPQ-27	Key Top	1		
KPQ-28	Key Top	1		

REF.NO.	DESCRIPTION	QTY	RS PART NO.	MFR's PART NO.
KPQ-29	Key Top 	1		
KPQ-30	Key Top 	1		
KPQ-31	Key Top	1		
KPQ-32	Key Top	1		
KPQ-33	Key Top	1		
KPQ-34	Key Top	1		
KPQ-35	Key Top	1		
KPQ-36	Key Top	1		
KPQ-37	Key Top	1		
KPQ-38	Key Top	1		
KPQ-39	Key Top	1		
KPQ-40	Key Top	1		
KPQ-41	Key Top	1		
KPQ-42	Key Top	1		
KPQ-43	Key Top, left 	1		
KPQ-44	Key Top	1		
KPQ-45	Key Top	1		
KPQ-46	Key Top	1		
KPQ-47	Key Top	1		
KPQ-48	Key Top	1		
KPQ-49	Key Top	1		
KQP-50	Key Top	1		
KPQ-51	Key Top	1		
KPQ-52	Key Top	1		
KPQ-53	Key Top	1		
KPQ-54	Key Top right 	1		

REF.NO.	DESCRIPTION	QTY	RS PART NO.	MFR's PART NO.
KPQ-55	Key Top	1		
KPQ-56	Key Top	1		
KPQ-57	Key Top	1		
KPQ-58	Space key 	1		
KPQ-59	Key Top	1		
KPQ-60	Key Top	1		
KPQ-61	Key Top	1		
KPQ-62	Key Top	1		

VII. PCB VIEWS

VII-1. Main PCB Top View

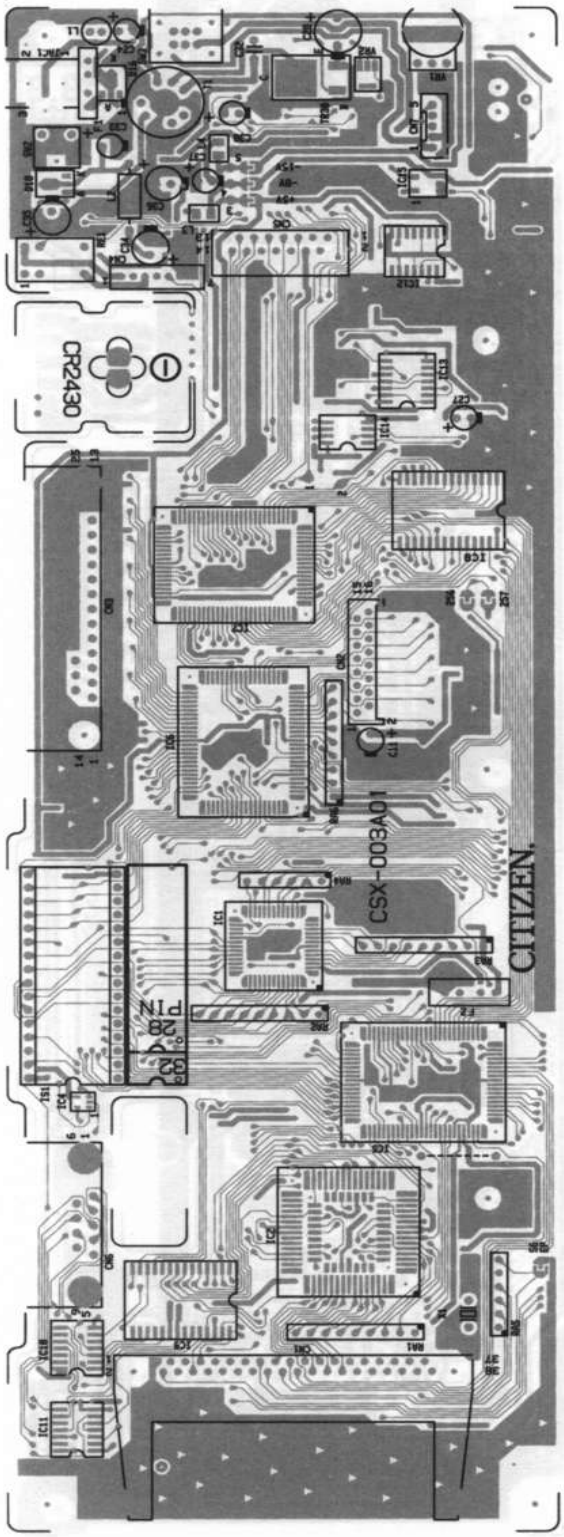


Figure 7-1. Main PCB Top View

VII-2. Main PCB Bottom View

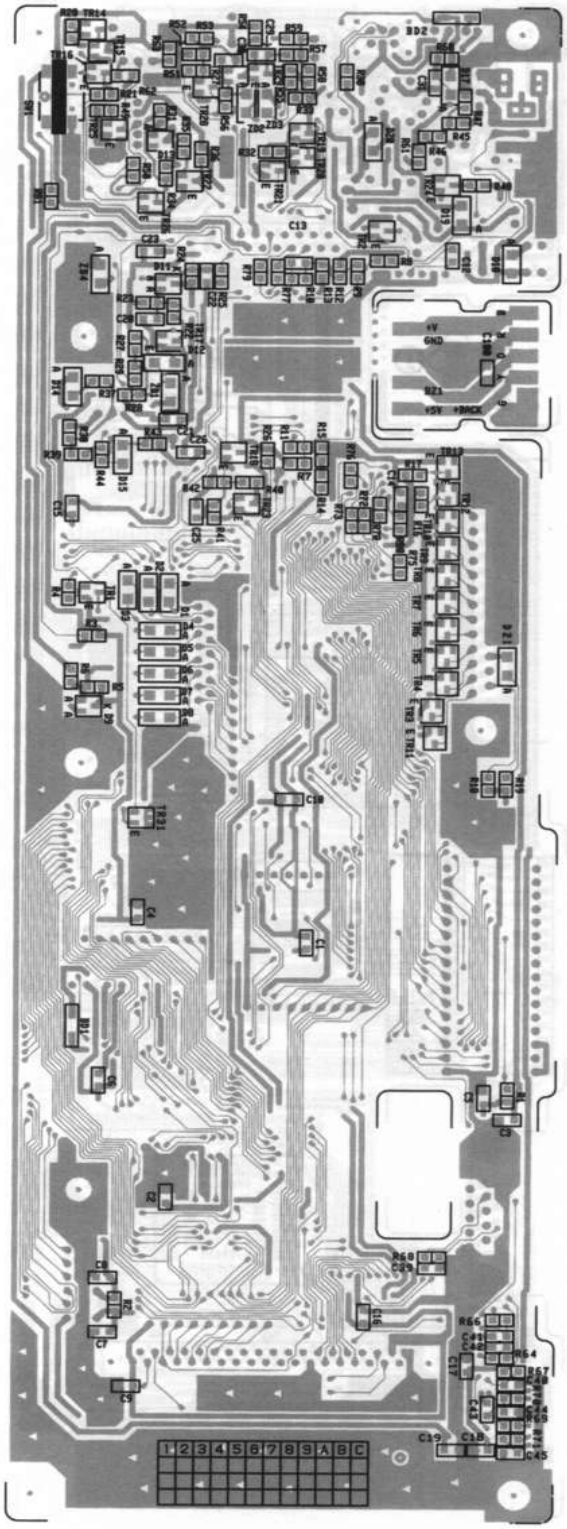


Figure 7-2. Main PCB Bottom View

VII-3. LCD PCB View

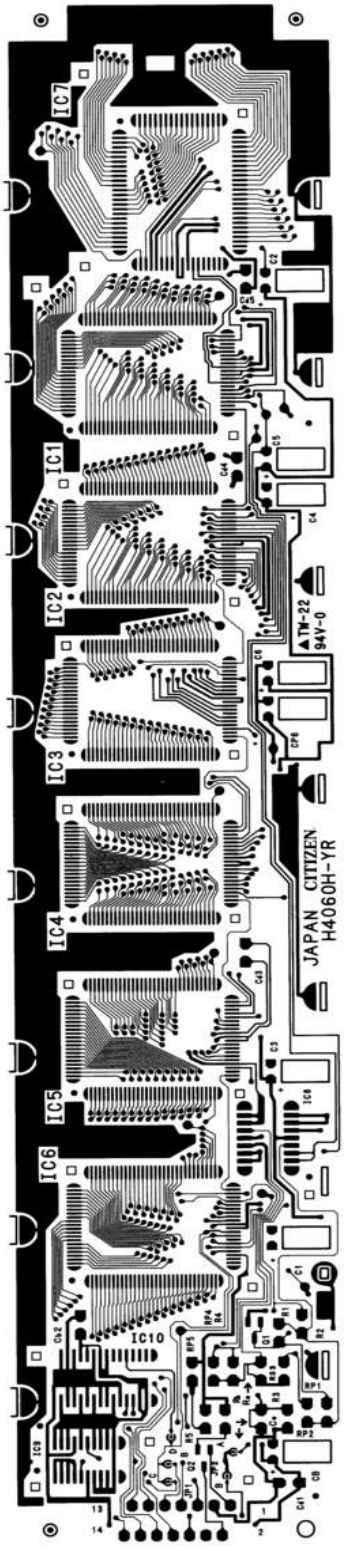
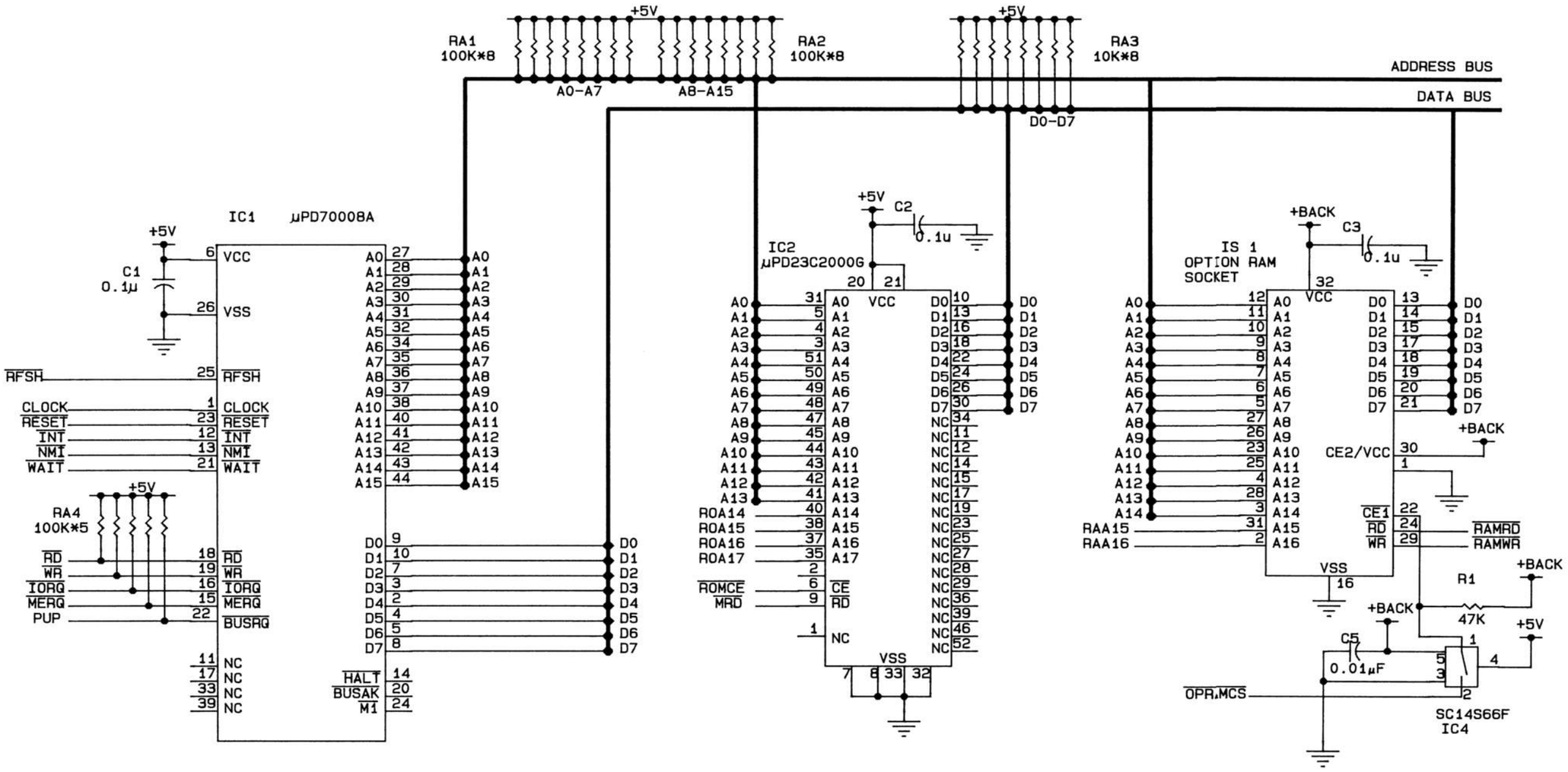


Figure 7-3. LCD PCB View

VIII. CIRCUIT DIAGRAMS

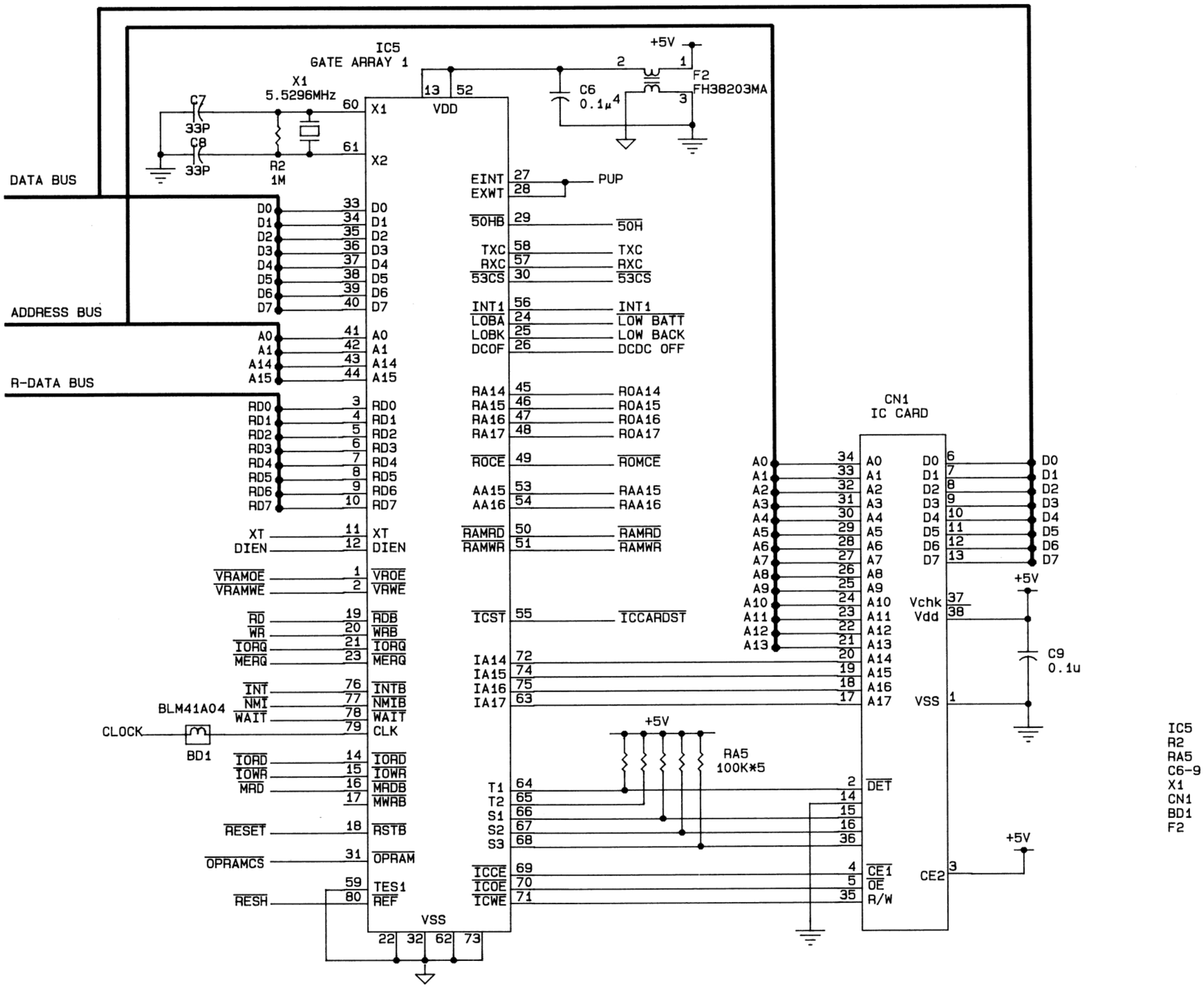
VIII-1. Main PCB Circuit Diagrams

CPU PART

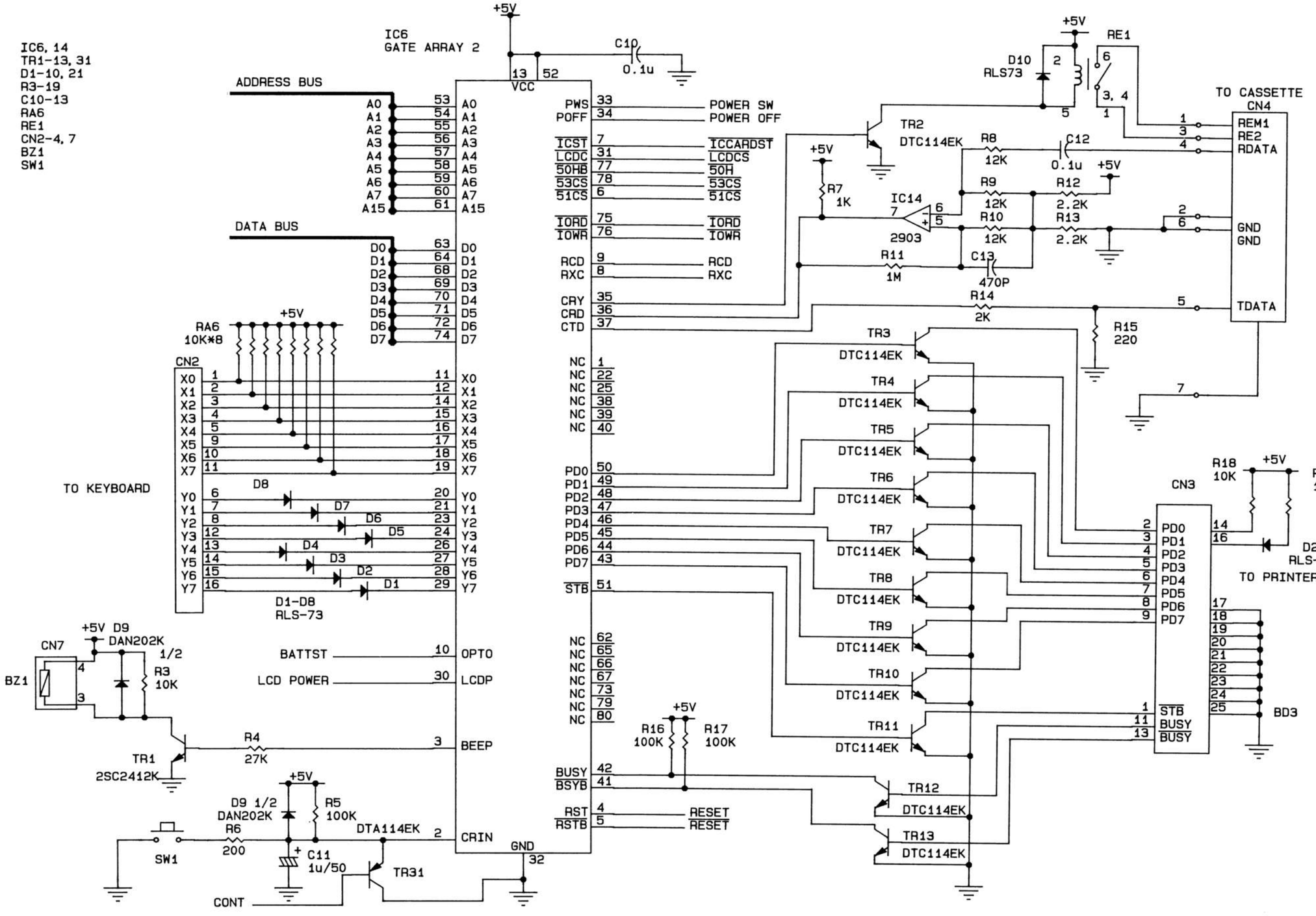


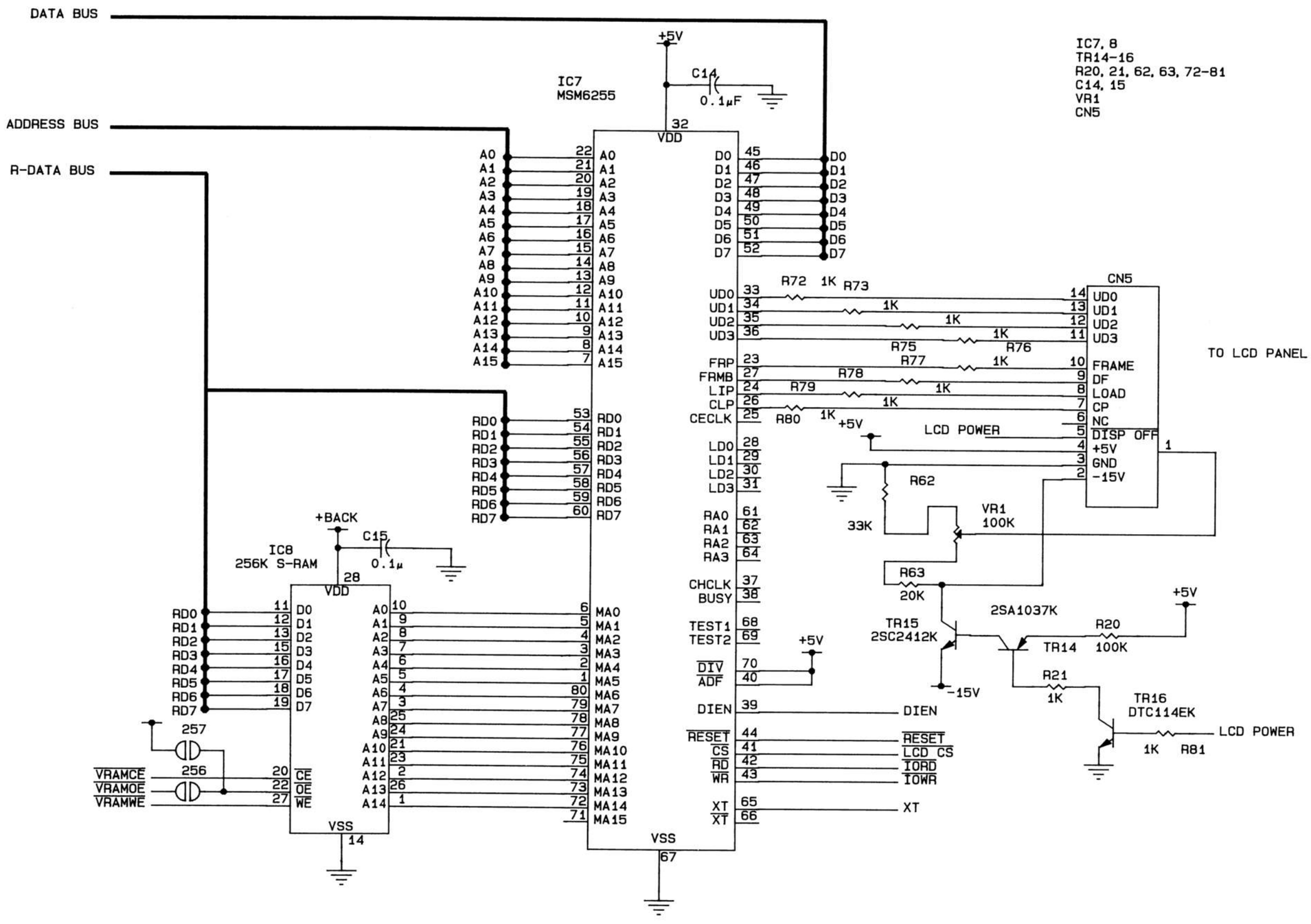
IC1, 2, 4
R1
C1-3, 5
RA1-4
IS 1

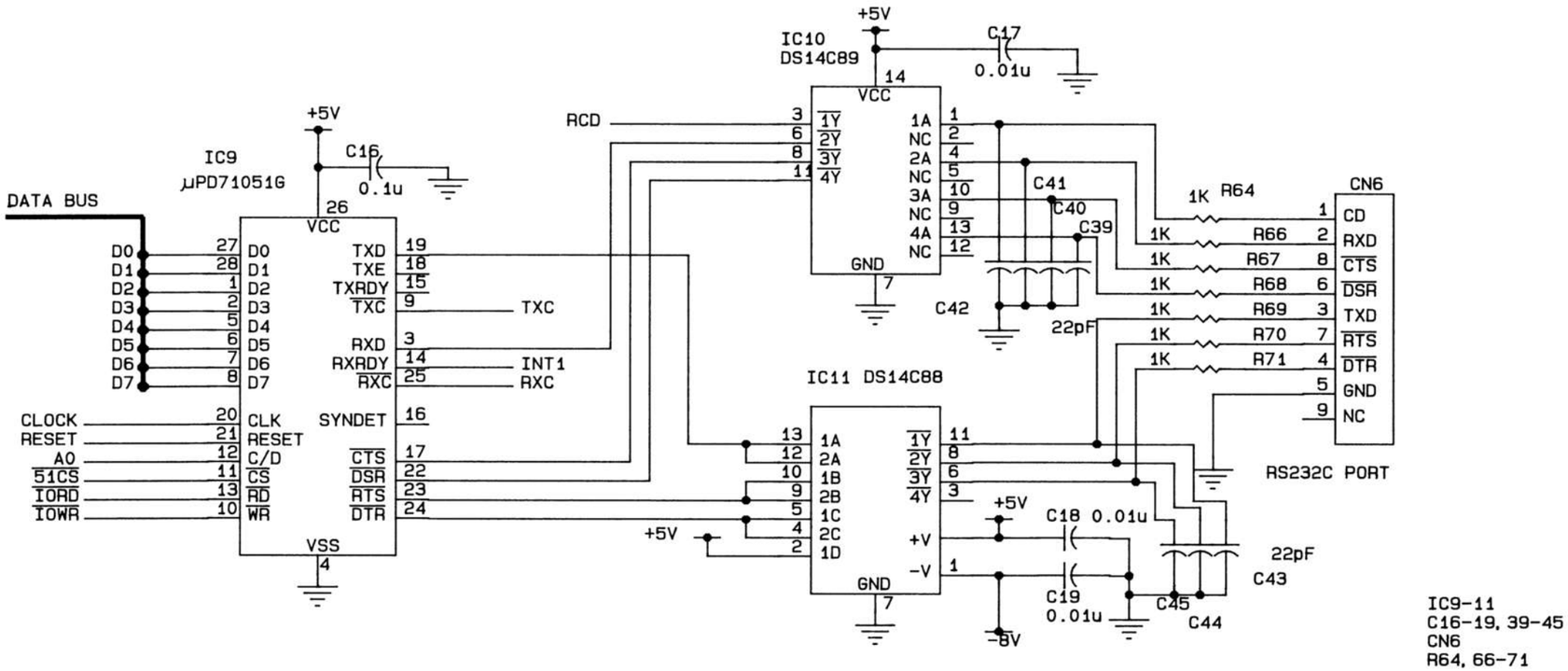
GATE ARRAY 1 & IC CARD



IC6, 14
TR1-13, 31
D1-10, 21
R3-19
C10-13
RA6
RE1
CN2-4, 7
BZ1
SW1

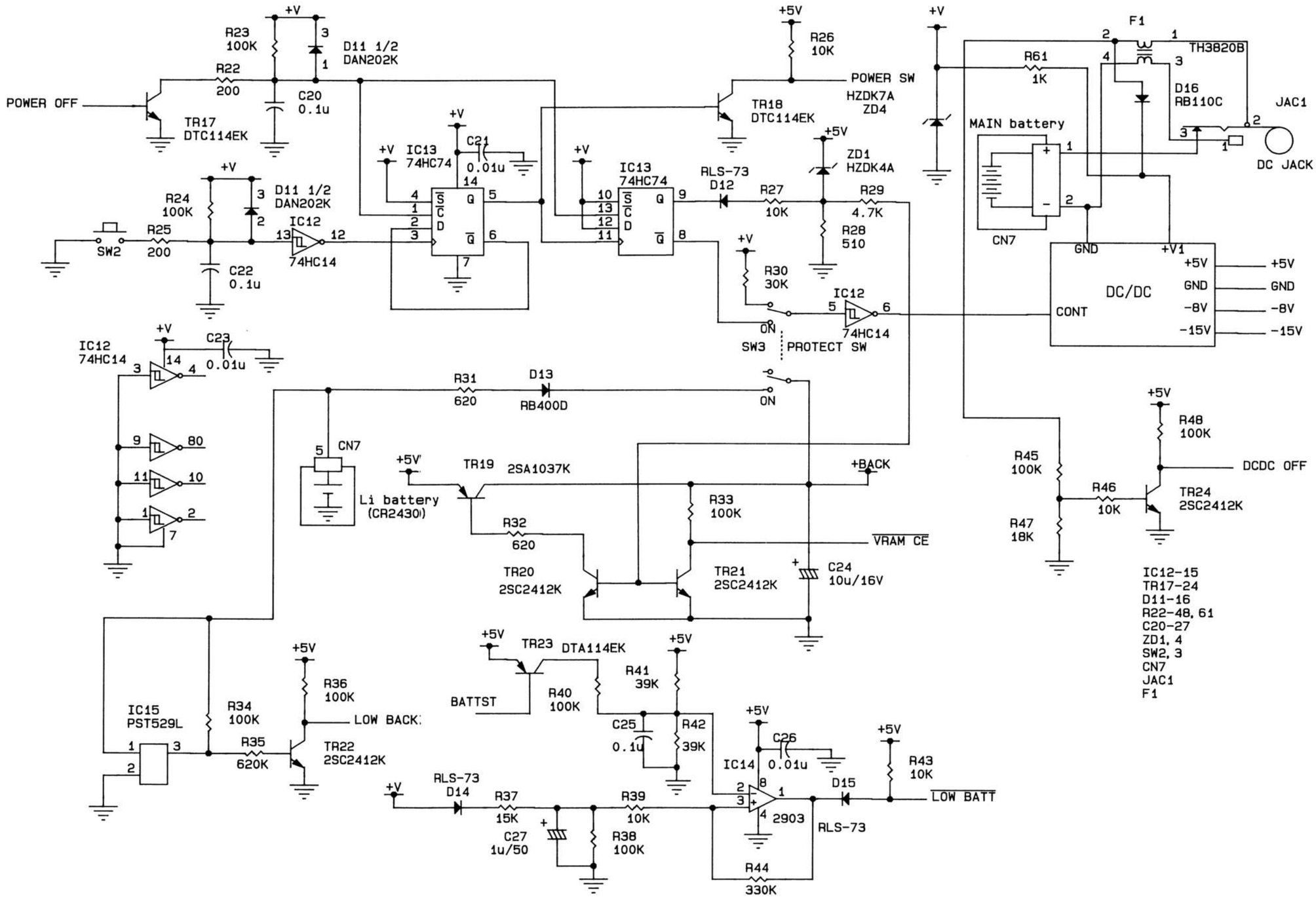



DATA BUS
ADDRESS BUS
R-DATA BUS
+5V
C14
0.1μF
IC7
MSM6255
32
VDD
IC7, 8
TR14-16
R20, 21, 62, 63, 72-81
C14, 15
VR1
CN5
A0 22 A0
A1 21 A1
A2 20 A2
A3 19 A3
A4 18 A4
A5 17 A5
A6 16 A6
A7 15 A7
A8 14 A8
A9 13 A9
A10 12 A10
A11 11 A11
A12 10 A12
A13 9 A13
A14 8 A14
A15 7 A15
D0 45 D0
D1 46 D1
D2 47 D2
D3 48 D3
D4 49 D4
D5 50 D5
D6 51 D6
D7 52 D7
RD0 53 RD0
RD1 54 RD1
RD2 55 RD2
RD3 56 RD3
RD4 57 RD4
RD5 58 RD5
RD6 59 RD6
RD7 60 RD7
R72 1K R73
UD0 33
UD1 34
UD2 35
UD3 36
1K
R75 R76
R77 1K
FRP 23
FRMB 27
R78
LIP 24
R79 1K
CLP 26
CECLK 25
R80 1K
LD0 28
LD1 29
LD2 30
LD3 31
RA0 61
RA1 62
RA2 63
RA3 64
CHCLK 37
BUSY 38
TEST1 68
TEST2 69
DIV 70
ADF 40
DIEN 39
RESET 44
CS 41
RD 42
WR 43
XT 65
XT 66
CN5
14 UD0
13 UD1
12 UD2
11 UD3
10 FRAME
9 DF
8 LOAD
7 CP
6 NC
5 DISP OFF
4 +5V
3 GND
2 -15V
1
TO LCD PANEL
+5V
LCD POWER
R62
33K
VR1
100K
R63
20K
2SA1037K
TR15
2SC2412K
TR14
R20
100K
R21
1K
TR16
DTC114EK
1K R81
LCD POWER
-15V
+5V
DIEN
RESET
LCD CS
IORD
IOWR
XT
+BACK
C15
0.1μ
IC8
256K S-RAM
28
VDD
RD0 11 D0
RD1 12 D1
RD2 13 D2
RD3 15 D3
RD4 16 D4
RD5 17 D5
RD6 18 D6
RD7 19 D7
A0 10 MA0
A1 9 MA1
A2 8 MA2
A3 7 MA3
A4 6 MA4
A5 5 MA5
A6 4 MA6
A7 3 MA7
A8 25 MA8
A9 24 MA9
A10 21 MA10
A11 23 MA11
A12 2 MA12
A13 26 MA13
A14 1 MA14
MA15 71
257
256
VRAMCE 20 CE
VRAMOE 22 OE
VRAMWE 27 WE
VSS 14
VSS 67



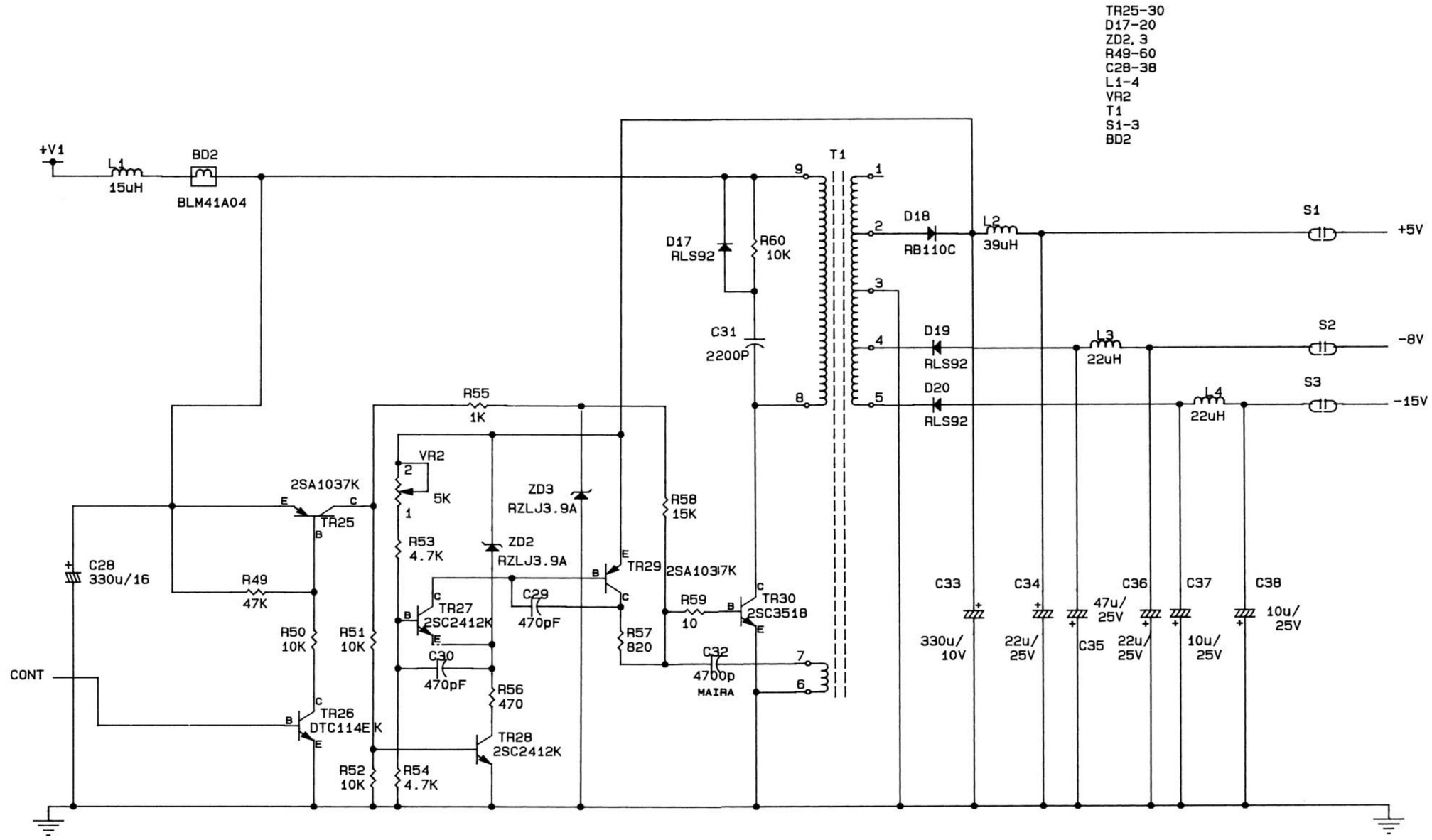
IC9-11
C16-19, 39-45
CN6
R64, 66-71

POWER CONTROL



IC12-15
TR17-24
D11-16
R22-48, 61
C20-27
ZD1, 4
SW2, 3
CN7
JAC1
F1

TR25-30
D17-20
ZD2, 3
R49-60
C28-38
L1-4
VR2
T1
S1-3
BD2



APPENDICIES

A. LCD SPECIFICATIONS

1. Application

These specifications shall be applied to Dot Matrix LCD MODULE H4060H-YR.

2. Composition

Display type	: STN, yellow mode, reflective positive display
Dot structure	: 480 × 64 Dot Graphic display
Driving method	: 1/64 duty Multiplex drive
Connector	: IL-FPC-14S-S1L1 (JAE)

Block Diagram

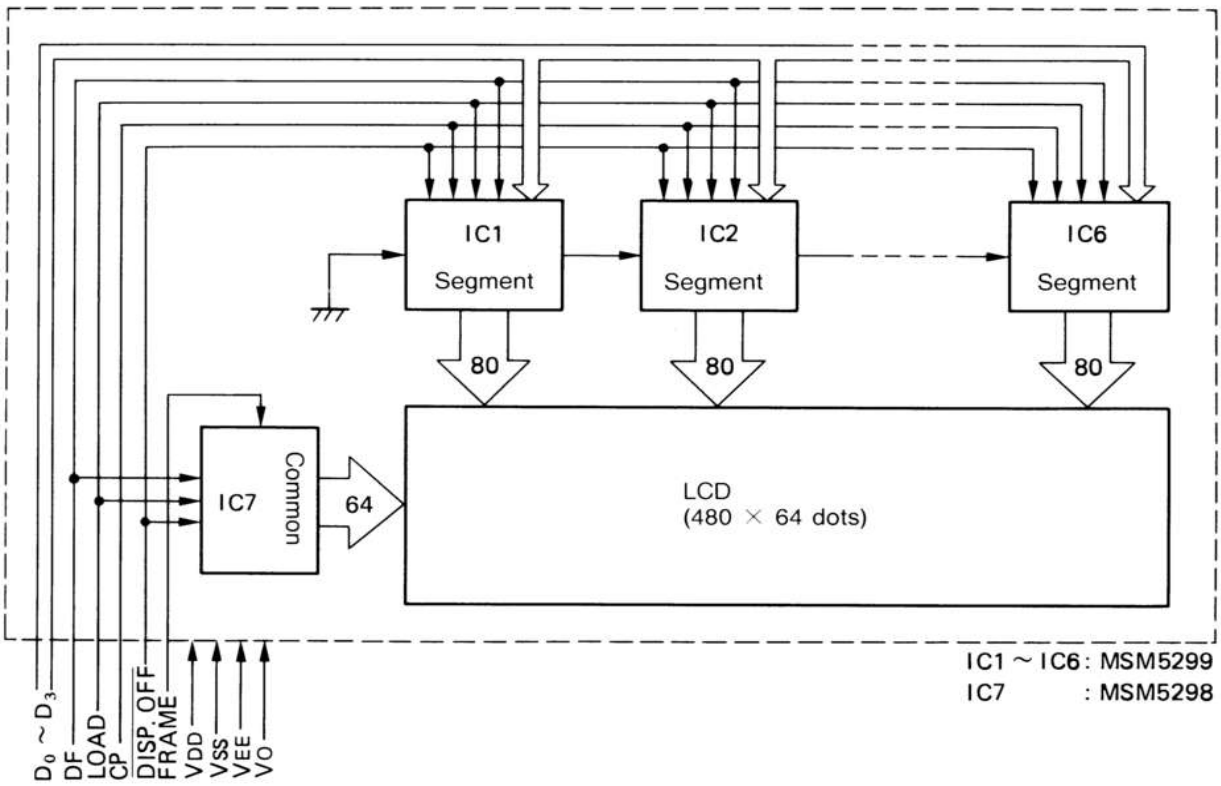


Figure A-1. Block Diagram

Note: This does not incorporate any controller.

3. Mechanical Specifications

Item	Dimensions	Unit
Module size	260 (W) × 52 (H) × 9.5 (D) max	mm
Effective viewing area	218 (W) × 36 (H)	mm
Weight	Approx. 150	g

Note: Module size [9.5 (D) max] does not include the connector.

Dot Dimensional Drawing (Unit mm)

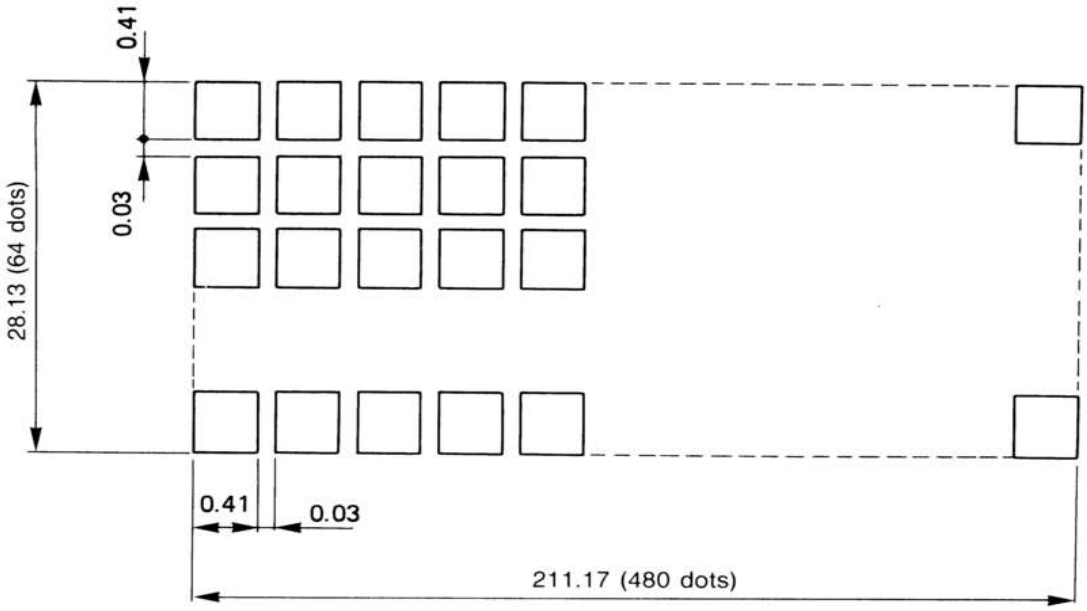


Figure A-2. Dot Dimensional Drawing

4. Electrical Specifications

4-1. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Remarks
Supply voltage for logic circuit	$V_{DD} - V_{SS}$	−0.3	+6.0	V	
Supply voltage for LCD driving	$V_{DD} - V_{EE}$	0	+30.0	V	
Input voltage	V_{IN}	−0.3	V_{DD}+0.3	V	
Storage temperature	T_{stg}	−20	+60	°C	
Operating temperature	T_{opr}	0	+40	°C	

4-2. Electrical Characteristics

Item	Symbol	Test condition	Min	Typ	Max	Unit
Supply voltage for logic circuit	$V_{DD} - V_{SS}$		4.5	5.0	5.5	V
Supply voltage for LCD driving	$V_{DD} - V_{EE}$		9.0	—	28.0	V
FRAME frequency	f_{FRAME}		—	70.0	—	Hz
Input voltage H level	V_{IH}	$V_{DD} - V_{SS}$=5.0V ±10%	0.8V_{DD}	—	V_{DD}	V
Input voltage L level	VIL		V_{SS}	—	0.2V_{DD}	V
Current consumption	I_{SS}	Ta=25°C $V_{DD} - V_{SS}$=5.0V $V_{DD} - V_{EE}$=14.3V	—	0.5	2.4	mA
	I_{EE}	$V_O = V_{EE}$ f_{FRAME}=70 Hz	—	2.3	4.7	mA

* $V_{DD} > V_{SS} > V_O \geqq V_{EE}$

4-3. Operating voltage for LCD driving

The contrast of the liquid crystal display depends on viewing angle, ambient temperature, and operating voltage, etc. Adjust the contrast by varying Vo as necessary.
The following values are recommended.

Ta=0°C..... 15.5Vtyp
Ta=25°C..... 14.3Vtyp $\theta = 0°, \phi = 0°$
Ta=40°C..... 13.7Vtyp

4-4. Vo adjusting circuit

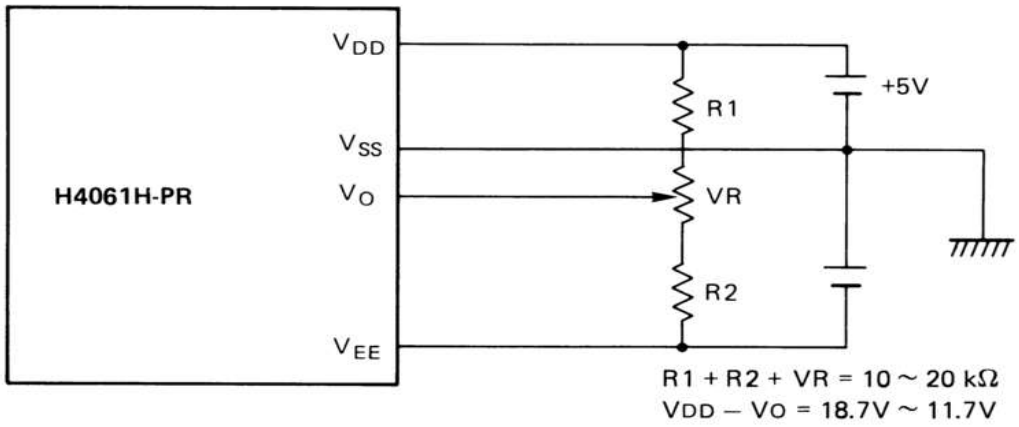


Figure A-3. Vo Adjusting Circuit

5. Interface Specifications

5-1. Terminal Pin Assignment

Pin No.	Symbol	Function
1	V_O	Operating Voltage for LCD driving
2	V_{EE}	Supply Voltage for LCD driving
3	V_{SS}	GND
4	V_{DD}	+5V (Supply voltage for logic circuit)
5	$\overline{\text{DISP. OFF}}$	Low level : LCD becomes non-visual. Hi level : LCD operates normally.
6	NC (FG)	No connection
7	CP	Shift register clock pulse for segment driver
8	LOAD	Signal for latching 1 line shift register DATA & commmon driver DATA shift signal
9	DF	A.C. signal for LCD driving
10	FRAME	Start signal of each display cycle (Shift register DATA signal of common driver)
11 – 14	D3 – D0	DATA Input signal (Fig. A-4)

5-2. Relationships of DATA Input Signal and LCD Screen Division

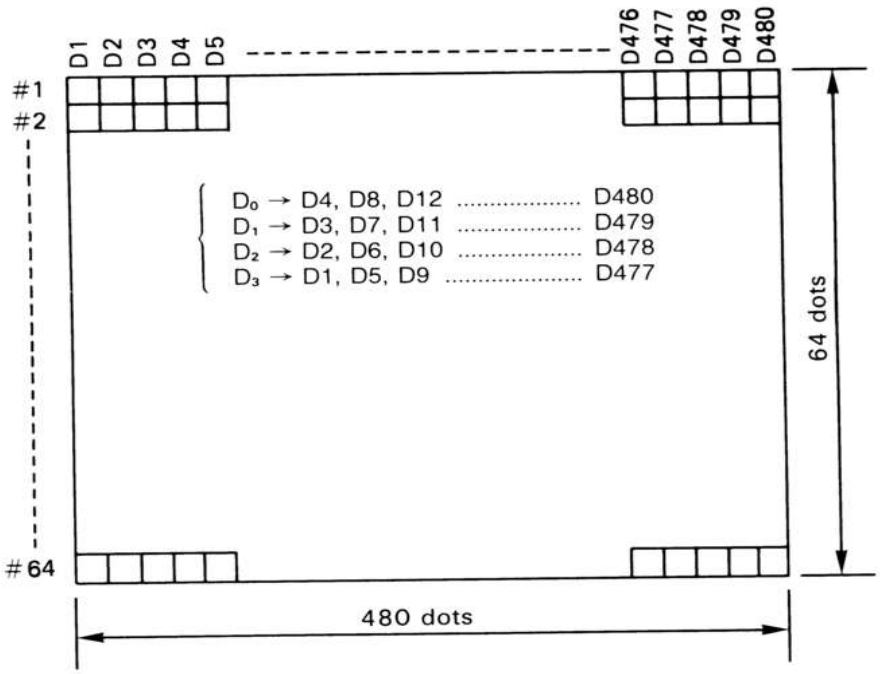


Figure A-4. LCD Screen

5-3. Timing Chart

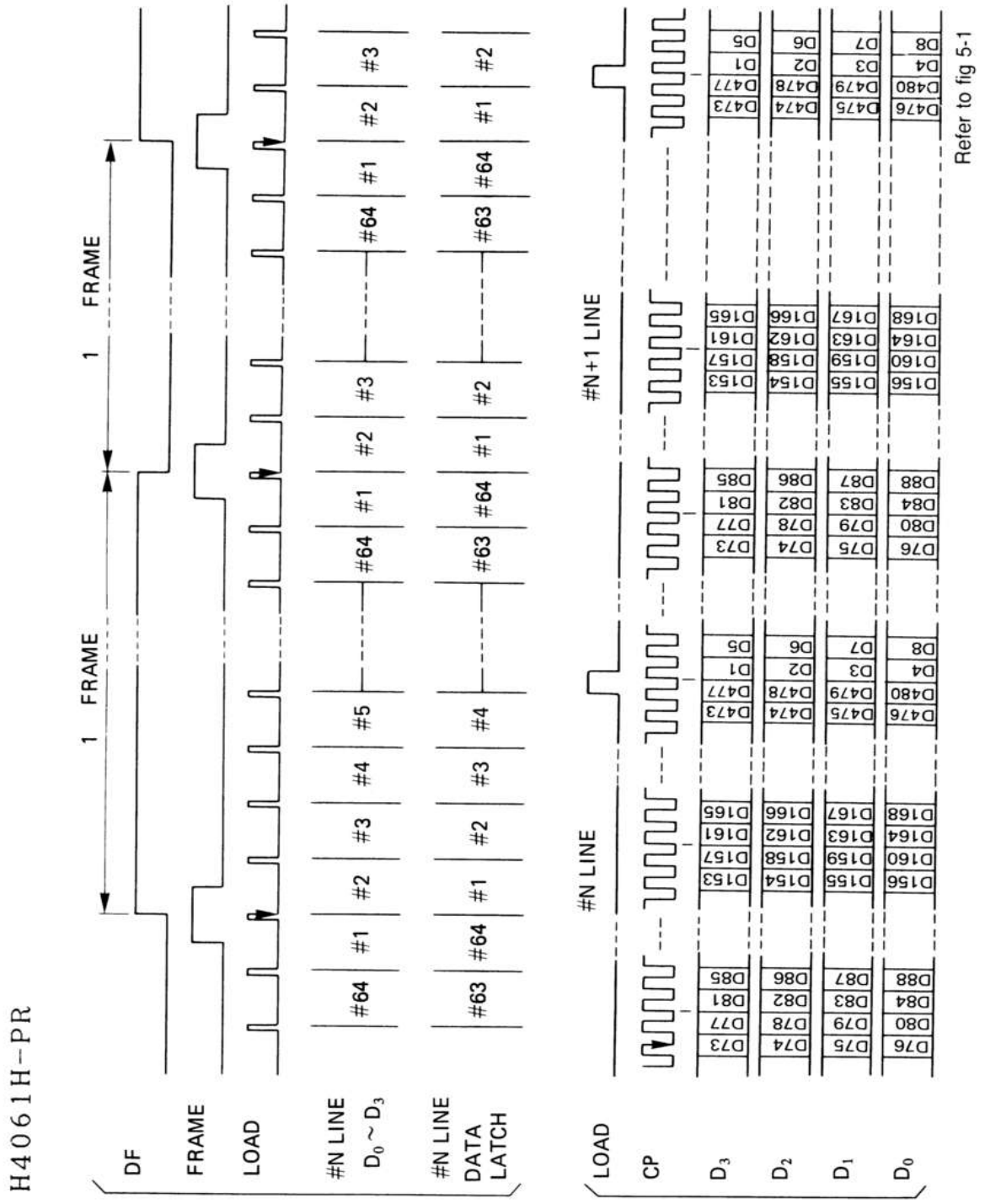


Figure A-5. Timing Chart

5-4. Switching Characteristics

V_{DD} = 5V ± 10%

Item	Symbol	Condition	Min	Typ	Max	Unit
CP frequency	f_{CP}	DUTY=50%	—	—	3	MHz
CP LOAD pulse width	tw	—	125	—	—	ns
DATA SET UP TIME D0 – D3 → CP	t_{OSU}	—	100	—	—	ns
LOAD SET UP TIME	t_{LSU}	—	125	—	—	ns
LOAD ←→ CP TIME	t_{LC}, t_a	—	200	—	—	ns
DATA HOLD TIME CP → D0 – D3	t_{DHD}	—	100	—	—	ns
LOAD → FRAME TIME	t_{LF}	—	300	—	—	ns
FRAME → LOAD TIME	t_{FL}	—	300	—	—	ns
FRAME SET UP TIME FRAME → LOAD	$t_{setup\ (FR)}$	—	100	—	—	ns
FRAME HOLD TIME LOAD → FRAME	$t_{hold\ (FR)}$	—	100	—	—	ns
LOAD ←→ DF DELAY TIME	t_{LD}	—	—	—	300	ns
CP RISE & FALL TIME	t r(CP) t f(CP)	—	—	—50	ns	
LOAD RISE & FALL TIME	t r(L) t f(L)	—	—	—	50	ns
DF RISE & FALL TIME	t r(DF) t f(DF)	—	—	—	100	ns

5-5. Input Capacitance

Signal	Input Capacitance	Unit
FRAME	15 Typ	pF
DF	40 Typ	pF
LOAD	45 Typ	pF
CP	35 Typ	pF
D3 – D0	35 Typ	pF

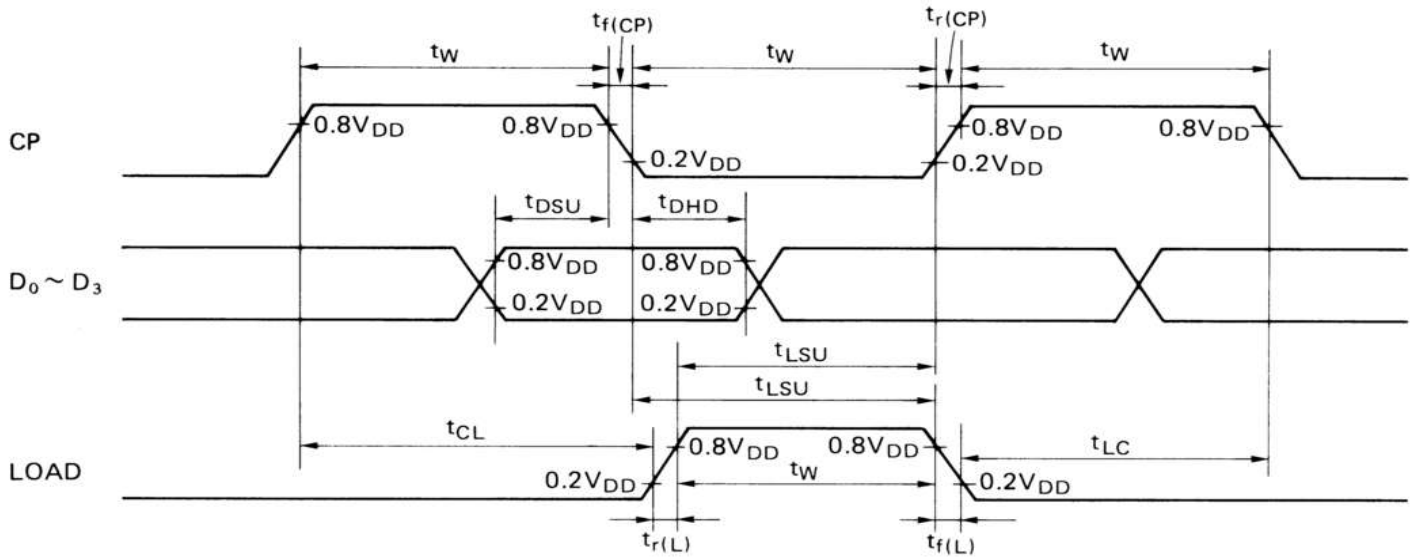


Figure A-6. Timing Chart

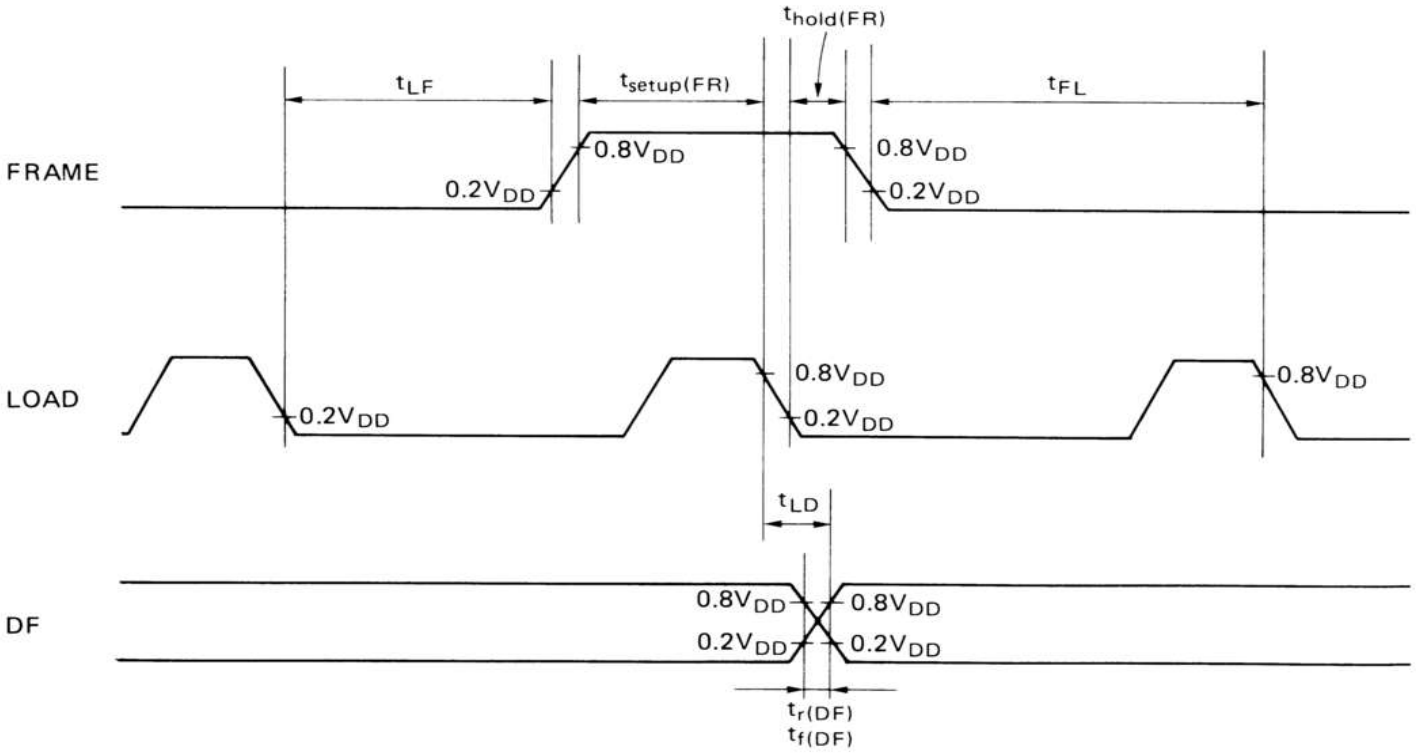


Figure A-7. Timing Chart

6. Optical Characteristics (refer to Note 1 – Note 4)

Ta = 25°C

Item	Symbol	Min	Typ	Max	Unit	Condition
Turn on time	t_{ON}	—	150	270	ms	$\theta=0°$, $\phi=0°$
Turn off time	t_{OFF}	—	200	360	ms	
Contrast ratio	CR	—		—		$\theta=0°$, $\phi=0°$
Visual angle range	$\theta 1$		$\leqq\theta 1\leqq$		deg.	$\theta=0°$, CR $\geqq$ 1.4
	$\theta 2$		$\leqq\theta 2\leqq$		deg.	$\theta=90°$, CR $\geqq$ 1.4

Note 1: Optical Characteristics measurement system

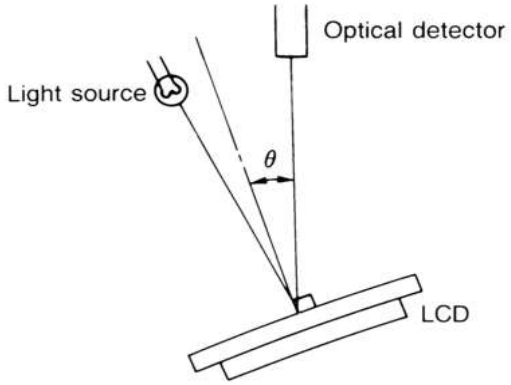


Figure A-8. Optical Characteristics Measurement System

Note 2: Definition of response time

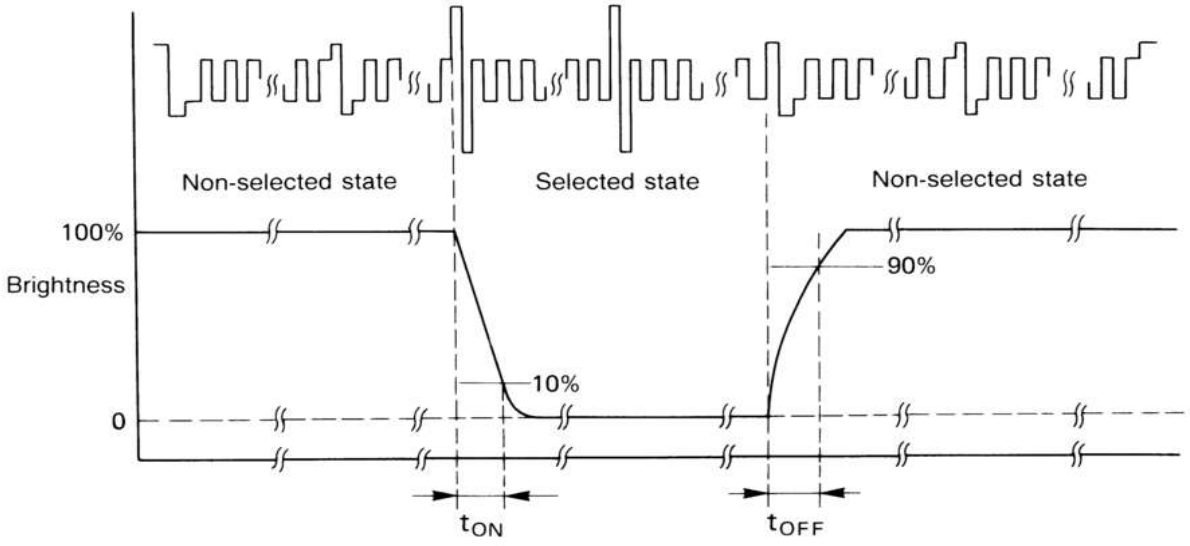


Figure A-9. Definition of Response Time

Note 3: Defintion of θ and ϕ

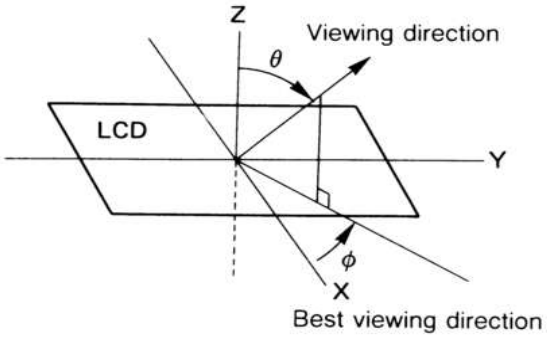


Figure A-10. Definition of θ and ϕ

Note 4: Definition of contrast ratio

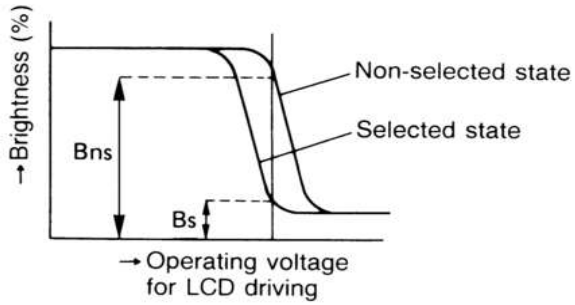


Figure A-11. Definition of Contrast Ratio

$$CR = \frac{\text{Brightness at selected state (Bs)}}{\text{Brightness at non-selected state (Bns)}}$$

7. Precautions in Use

7-1. Precautions for handling

(1) The polarizer is quite susceptible to scratches. Handle it very carefully. Do not handle it with metallic tweezers. Do not press it or rub it.
(2) Do not touch the display face or stain it.
If the surface is dirty, wipe it off lightly with a cotton swab or a piece of soft cloth or chamois which is soaked with petroleum or benzine. Never use organic solvents including acetone, toluene, ethanol, and isopropyl alcohol: they would damage the surface.
(3) Do not allow saliva or water to remain on the surface for long; it might cause a local deformation or discoloration.
(4) If the LCD breaks and the liquid crystal comes out, never put it in your mouth. If it sticks to the skin or clothes, wash it off with soap immediately.

7-2. Installation

(1) The ICs mounted on the PCB are very susceptible to static electricity. To protect them from static electricity which your body and clothing collect, connect your body to ground via a resistor of some 1M ohms to discharge electricity. Connect the resistor close to your body in the grounding line and protect yourself from electric shock hazard.
(2) Do not bend or twist the module excessively when installing it. If you do, the device might break or the circuits might fail.
(3) Protect the LCD, particularly the surface of the polarizer, with a transparent plate (such as an acrylic or glass plate) on the cabinet.

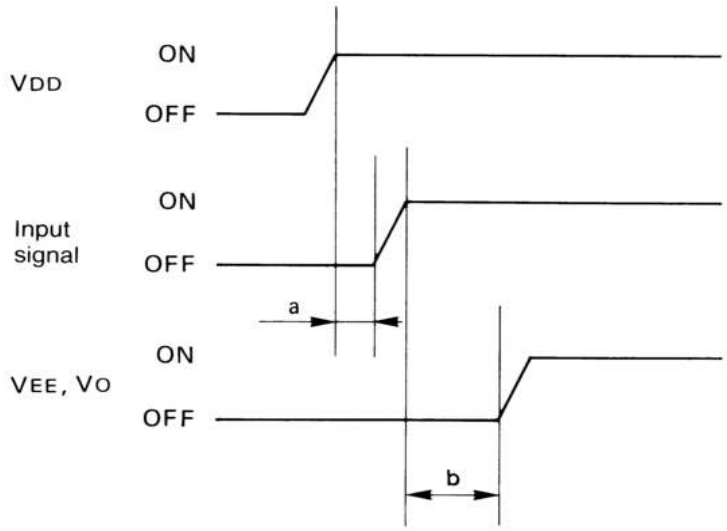
7-3. Storage

(1) Avoid high temperature and high humidity. The temperature should be 0 – 35°C and humidity under 60%.
(2) Store the module in a dark place, out of direct sunlight and fluorescent light, etc.
(3) Keep the polarizer away from any external forces.
(4) Store the module in the box when shipping it.

7-4. Operational precautions

(1) The ICs will break down if the drive voltage exceeds the limit. Make sure of electrical specifications, particularly the supply voltage.
(2) The response of the display is slow when the ambient temperature is below the lower limit, and the display becomes unusual when the ambient temperature is above the upper limit. In any case, it does not mean failure. It operates properly in the normal operating temperature range.
(3) The contrast of the liquid crystal varies with the viewing angle, ambient temperature, and drive voltage. Adjust the drive voltage for the best contrast by installing an external variable switch.
(4) If you move the module from cold storage into a room, as during a test, moisture would condense on the module and it might fail.
(5) In order to prevent IC Latch-up and DC voltage on the LCD panel, turn power on by following Figure A-12.

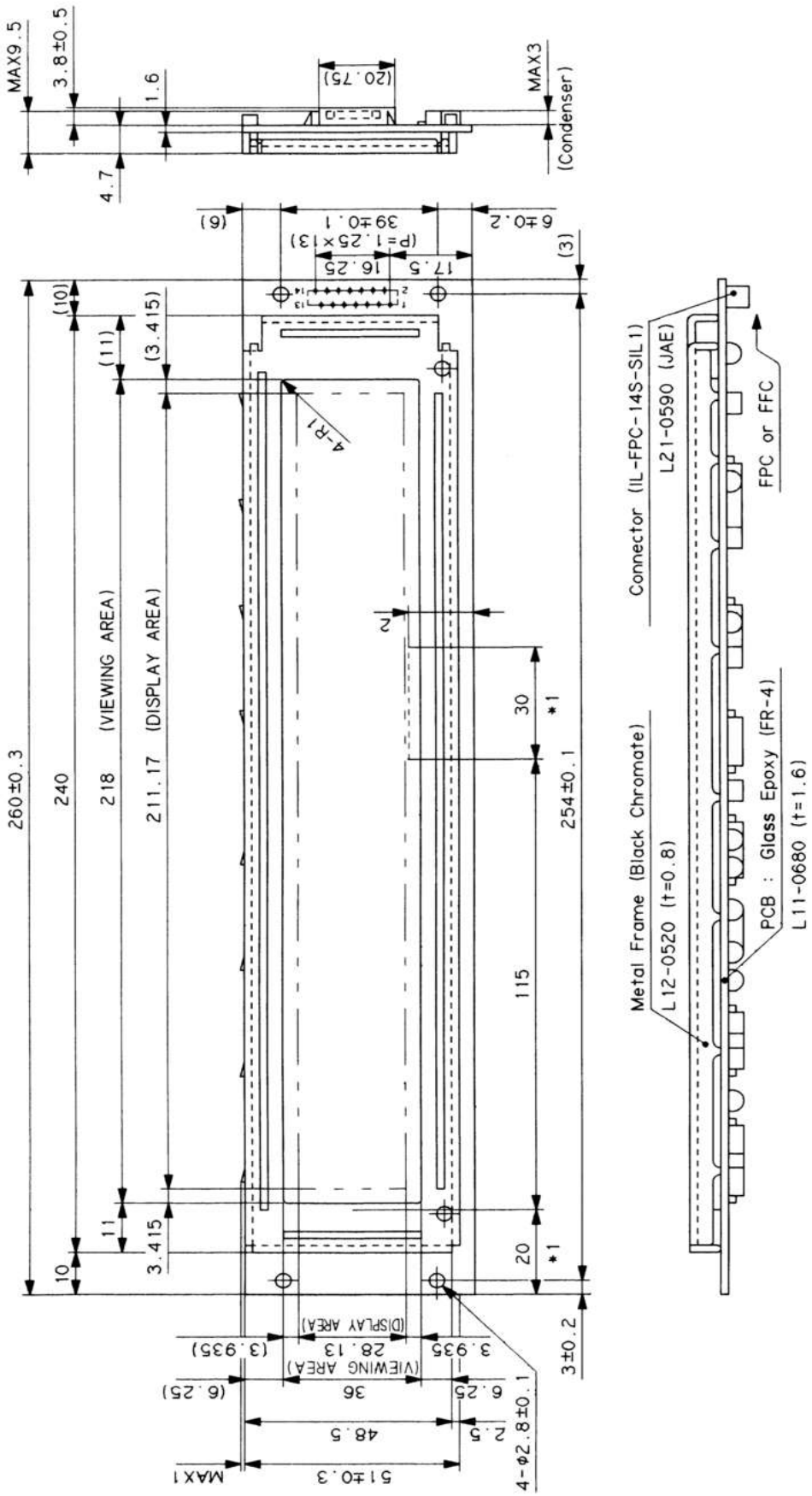
Note: FRAME frequency = 70 Hz



Note: FRAME frequency = 70 Hz

Figure A-12. Operational Precautions

8. LCD Module View



B. INSTALLATION OF OPTIONAL RAM

1. Turn off the back-up battery switch.

2. Remove 5 screws "A" from the lower case.
   Refer to Figure 2-3. Top Case Removal

3. Remove the upper case.
   The upper and lower cases are secured by snaps. Pull up the front of the upper case first, as shown in Figure 2-1. Do not apply too much force when pulling it.

4. Disconnect the LCD flat cable from the connector on the main PCB.
   Refer to Figure 2-4. LCD Cable Removal.

5. Insert the optional RAM into the IC socket marked IS1.
   Refer to Figure B-1. RAM Insertion.

6. Press [F2]-[Ctrl]-[Bs] or Reset Switch (SW2) after power on.

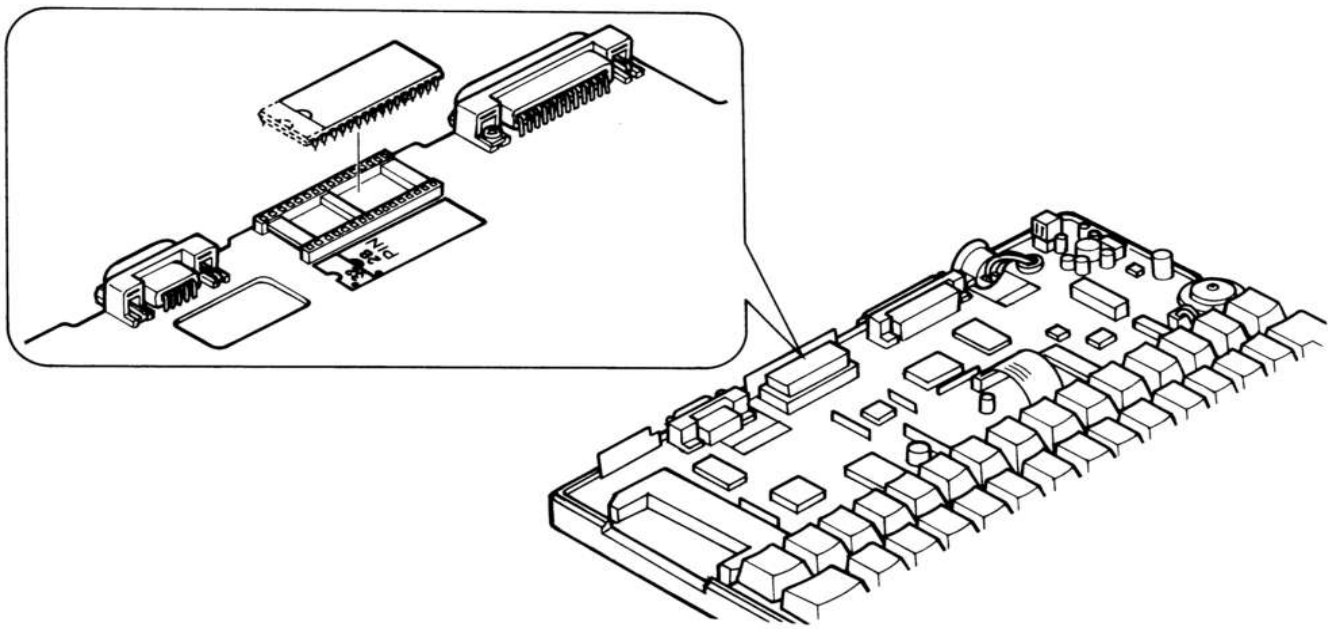
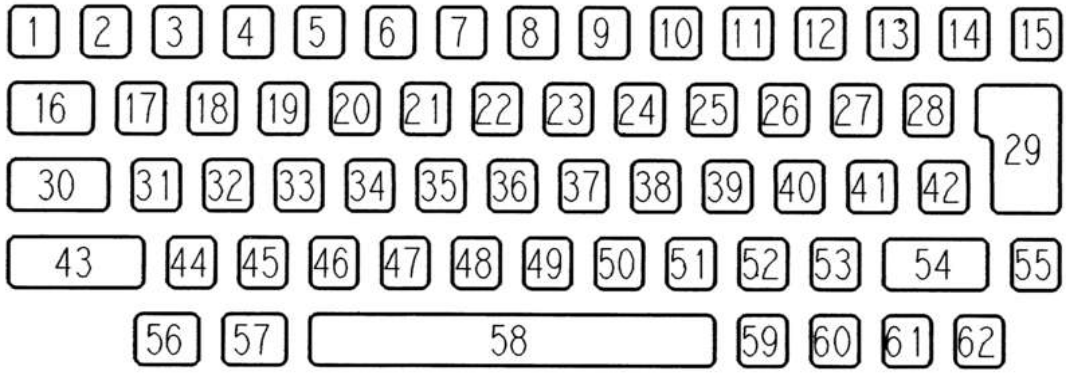
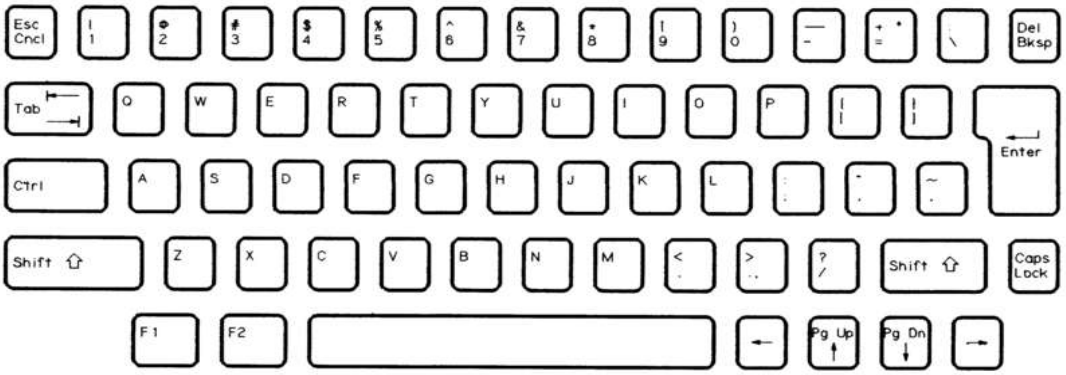


Figure B-1. RAM Insertion

C. KEYBOARD LAYOUT, CONNECTOR PIN ASSIGNMENTS, AND CHARACTER CODE TABLES

1. Keyboard Layout





Figures C-1, C-2. Keyboard Layout

2. Connector Pin Assignments

RS-232-C Interface (Table C-1)

Pin No.	Symbol	Description
1	CD	Carrier detect
2	RXD	Receive data
3	TXD	Transmit data
4	DTR	Data terminal ready
5	GND	
6	DSR	Data-set ready
7	RTS	Request to send
8	CTS	Clear to send
9	NC	

Cassette Interface (Table C-2)

Pin No.	Symbol	Description
1	REM1	Remote
2	GND	
3	REM2	Remote
4	RXC	Receive data for CMT
5	TXC	Transmit data for CMT
6	GND	
7	NC	
8	NC	

Input level: Impedance 100 ohm (800 mV-50 Vp-p)
Output level: Impedance 3.3 Kohm (600 mVp-p $\pm$10%)
REMote: 6V DC 0.5A max

Printer Interface (Table C-3)

Pin No.	Symbol	Description
1	/STROBE	Strobe pulse from the WP-2 to printer.
2	PD0	Bit 0 (1sb) of output data byte
3	PD1	Bit 1 of output data byte
4	PD2	Bit 2 of output data byte
5	PD3	Bit 3 of output data byte
6	PD4	Bit 4 of output data byte
7	PD5	Bit 5 of output data byte
8	PD6	Bit 6 of output data byte
9	PD7	Bit 7 of output data byte
10	NC	
11	BUSY	Input to the WP-2 from printer, high signal indicates that printer is not ready.
12	NC	
13	/BUSY	Input to WP-2 from printer
14	/INIT	Pull up to +5V
15	NC	
16	/AUTOFD	Pull up to +5V
17	GND	
18	GND	
19	GND	
20	GND	
21	GND	
22	GND	
23	GND	
24	GND	
25	GND	

Expansion Card Interface (Table C-4)

Pin No.	Symbol	Description
1	GND	
2	+5V	Pull up to +5V
3		Chip enable 2 (pull up to +5V)
4	/ICCE	Chip enable 1
5	/ICOE	Output enable
6	D0	
7	D1	
8	D2	
9	D3	
10	D4	
11	D5	
12	D6	
13	D7	
14	GND	
15	+5V	Pull up to +5V
16	+5V	Pull up to +5V
17	IA17	Address 17 of IC Card
18	IA16	Address 16 of IC Card
19	IA15	Address 15 of IC Card
20	IA14	Address 14 of IC Card
21	A13	
22	A12	
23	A11	
24	A10	
25	A9	
26	A8	
27	A7	
28	A6	
29	A5	
30	A4	
31	A3	
32	A2	
33	A1	
34	A0	
35	/ICWE	IC Card write
36	+5V	Pull up to +5V
37	NC	
38	VDD	+5V supply

RS-232-C

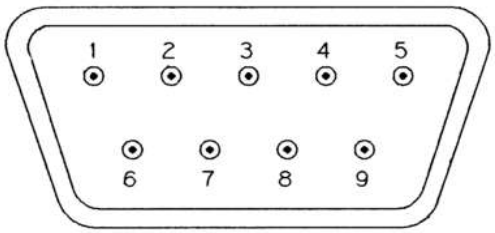


Figure C-1. RS-232C Interface

Cassette

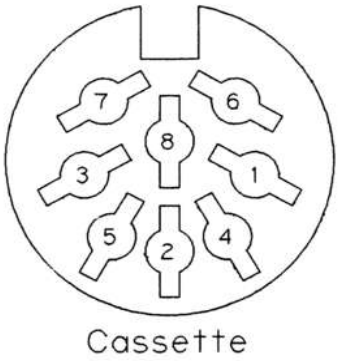


Figure C-4. Cassette Connector

Printer

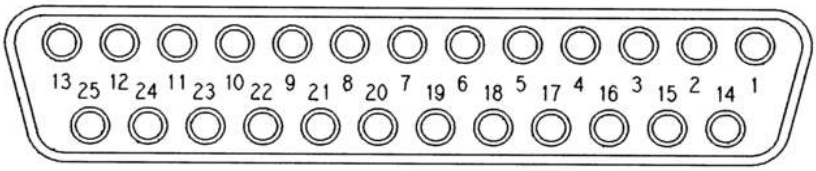


Figure C-5. Printer Connector

Expansion Card

Figure C-6. Expansion Card Connector

3. Character Code Tables

Table 1 ASCII Codes (Table C-5)

* Caps Lock is unlocked, GRPH/CODE is off

Decimal	Hex	Com.	Display character	Keyboard character
00	00	nul		
01	01			
02	02			
03	03			
04	04			
05	05			
06	06			
07	07			
08	08	BKSP		[BKSP]
09	09			
10	0A			
11	0B	Tab		[Tab]
12	0C			
13	0D	Enter		[Enter]
14	0E			
15	0F			
16	10			
17	11			
18	12			
19	13			
20	14			
21	15			
22	16			
23	17			
24	18			
25	19			
26	1A			
27	1B	Cncl		[Cncl]
28	1C			Right arrow
29	1D			Left arrow
30	1E			Up arrow
31	1F			Down arrow
32	20			[Space]
33	21		!	Shift 1
34	22		"	Shift '
35	23		#	Shift 3
36	24		$	Shift 4
37	25		%	Shift 5
38	26		&	Shift 7
39	27		'	'
40	28		(	Shift 9
41	29		)	Shift 0
42	2A		*	Shift 8
43	2B		+	Shift =
44	2C		,	,
45	2D		-	-
46	2E		.	.
47	2F		/	/
48	30		0	0
49	31		1	1
50	32		2	2
51	33		3	3
52	34		4	4

Decimal	Hex	Com.	Display character	Keyboard character
53	35		5	5
54	36		6	6
55	37		7	7
56	38		8	8
57	39		9	9
58	3A		:	Shift ;
59	3B		;	;
60	3C		<	Shift ,
61	3D		=	=
62	3E		>	Shift .
63	3F		?	Shift /
64	40		@	Shift 2
65	41		A	Shift A
66	42		B	Shift B
67	43		C	Shift C
68	44		D	Shift D
69	45		E	Shift E
70	46		F	Shift F
71	47		G	Shift G
72	48		H	Shift H
73	49		I	Shift I
74	4A		J	Shift J
75	4B		K	Shift K
76	4C		L	Shift L
77	4D		M	Shift M
78	4E		N	Shift N
79	4F		O	Shift O
80	50		P	Shift P
81	51		Q	Shift Q
82	52		R	Shift R
83	53		S	Shift S
84	54		T	Shift T
85	55		U	Shift U
86	56		V	Shift V
87	57		W	Shift W
88	58		X	Shift X
89	59		Y	Shift Y
90	5A		Z	Shift Z
91	5B		[	[
92	5C		\	\
93	5D		]	]
94	5E		^	Shift 6
95	5F		–	Shift –
96	60			
97	61		a	A
98	62		b	B
99	63		c	C
100	64		d	D
101	65		e	E
102	66		f	F
103	67		g	G
104	68		h	H
105	69		i	I
106	6A		j	J
107	6B		k	K
108	6C		l	L
109	6D		m	M

Decimal	Hex	Com.	Display character	Keyboard character
110	6E		n	N
111	6F		o	O
112	70		p	P
113	71		q	Q
114	72		r	R
115	73		s	S
116	74		t	T
117	75		u	U
118	76		v	V
119	77		w	W
120	78		x	X
121	79		y	Y
122	7A		z	Z
123	7B		{	Shift [
124	7C		|	Shift \
125	7D		}	Shift]
126	7E			
127	7F	Delete		Shift [BKSP]

* GRPH mode is on (By pressing [F1]-[Caps Lock])

Decimal	Hex	Com.	Display character	Keyboard character
00	00	nul	Space	
01	01		☺	A
02	02		☻	S
03	03		♥	Y
04	04		♦	H
05	05		♣	G
06	06		♠	J
07	07		•	`
08	08		◘	Shift '
09	09		○	P
10	0A		◙	Shift P
11	0B		♂	K
12	0C		♀	Shift K
13	0D		♪	;
14	0E		♫	Shift ;
15	0F		☼	Shift C
16	10		►	.
17	11		◄	,
18	12		↕	I
19	13		‼	Shift 1
20	14		¶	9
21	15		§	4
22	16		▬	
23	17		↨	Shift I
24	18		↑	Shift M
25	19		↓	Shift /
26	1A		→	Shift .
27	1B		←	Shift ,
28	1C		∟	=
29	1D		↔	-
30	1E		▲	M
31	1F		▼	/
32	20		SPACE	Shift [BKSP]
176	B0		⣿	[
177	B1		⣿	]
178	B2		⣿	¥
179	B3		┬	F
180	B4		┬	U
181	B5		┬	O
182	B6		┬	Shift O
183	B7		┬	Shift 0
184	B8		┬	0
185	B9		┬	Shift U
186	BA		┬	Shift F
187	BB		┬	Shift 8
188	BC		┬	Shift N
189	BD		┬	Shift L
190	BE		┬	L
191	BF		┬	8
192	C0		┴	V
193	C1		┴	B
194	C2		┴	6
195	C3		┴	R
196	C4		─	7
197	C5		┼	T

Decimal	Hex	Com.	Display character	Keyboard character
198	C6		╞	Q
199	C7		╟	Shift Q
200	C8		╚	Shift V
201	C9		╔	Shift 5
202	CA		╩	Shift B
203	CB		╦	Shift 6
204	CC		╠	Shift R
205	CD		═	Shift 7
206	CE		╬	Shift T
207	CF		╧	X
208	D0		╨	Shift X
209	D1		╤	3
210	D2		╥	Shift 3
211	D3		╙	Shift Z
212	D4		╘	Z
213	D5		╒	2
214	D6		╓	Shift 2
215	D7		╫	Shift W
216	D8		╪	W
217	D9		┘	N
218	DA		┌	5
219	DB		▉	C
220	DC		▄	E
221	DD		▌	D
222	DE		▐	Shift D
223	DF		▀	Shift E
254	FE		■	Shift‘

* CODE mode is on (By pressing [F2]-[Caps Lock])

Decimal	Hex	Com.	Display character	Keyboard character
128	80		Ç	Shift C
129	81		ü	J
130	82		é	3
131	83		â	1
132	84		ä	Q
133	85		à	A
134	86		å	Z
135	87		ç	C
136	88		ê	4
137	89		ë	D
138	8A		è	E
139	8B		ï	K
140	8C		î	9
141	8D		ì	I
142	8E		Ä	Shift Q
143	8F		Å	Shift Z
144	90		É	Shift 3
145	91		æ	W
146	92		Æ	Shift W
147	93		ô	0
148	94		ö	L
149	95		ò	O
150	96		û	8
151	97		ù	U
152	98		ÿ	Shift Y
153	99		Ö	Shift L
154	9A		Ü	Shift J
155	9B		¢	'
156	9C		£	Y
157	9D		¥	\
158	9E		Pt	P
159	9F		*f*	Shift P
160	A0		á	Shift A
161	A1		í	Shift I
162	A2		ó	Shift O
163	A3		ú	Shift U
164	A4		ñ	N
165	A5		Ñ	Shift N
166	A6		a	-
167	A7		o	Shift -
168	A8		¿	Shift /
169	A9		⌐	[
170	AA		¬	]
171	AB		½	V
172	AC		¼	Shift V
173	AD		¡	Shift 1
174	AE		«	,
175	AF		»	.
224	E0		α	G
225	E1		β	B
226	E2		Γ	R
227	E3		π	X
228	E4		Σ	S
229	E5		σ	7
230	E6		μ	Shift 8

Decimal	Hex	Com.	Display character	Keyboard character
231	E7		γ	Shift R
232	E8		Φ	Shift G
233	E9		θ	Shift H
234	EA		Ω	H
235	EB		δ	Shift 7
236	EC		∞	Shift X
237	ED		ϕ	;
238	EE		ϵ	Shift 6
239	EF		$\cap$	6
240	F0		$\equiv$	=
241	F1		$\pm$	Shift =
242	F2		$\geq$	Shift .
243	F3		$\leq$	Shift ,
244	F4		⌠	Shift F
245	F5		⌡	F
246	F6		$\div$	/
247	F7		$\approx$	‘
248	F8		$^\circ$	T
249	F9		$\bullet$	Shift T
250	FA		-	M
251	FB		$\surd$	5
252	FC		^{n}	Shift 2
253	FD		^{2}	2

Table. ESC Sequence Code (VT52) (Table C-6)

Escape Sequence	Function
ESC A	Cursor Up
ESC B	Cursor Down
ESC C	Cursor Right
ESC D	Cursor Left
ESC H	Cursor to Home
ESC J	Erase to End of Screen
ESC K	Erase to End of Line
ESC Y Line column	Direct Cursor Address
ESC Z	Identify

D. ROM CALLS AND SPELLER INFORMATION

1. ROM CALLS

CHARSENSE =	Check keyboard buffer
ENTRY:	0100H
ENTER:	Nothing
EXIT:	Zero flag set = no key Zero flag reset = key exists H =character code L =control key status bit 0: F2 bit 1: F1 bit 2: Ctrl bit 3: Shift (right) bit 4: Shift (left) bit 5: Caps Lock OFF/ON bit 7,6 0,x: normal mode 1,0: GRPH mode 1,1: CODE mode Carry flag set =ASCII character Carry flag reset=CODE or GRAPH CHARACTER
REGISTERS PRESERVED	BC,DE,IX,IY AF',BC',DE',HL'
CHARGET =	Get one character (wait for input if none in key-buffer)
ENTRY:	0103H
ENTER:	Nothing
EXIT:	Zero flag set = no key Zero flag reset = key exists H =character code L =control key status bit 0: F2 bit 1: F1 bit 2: Ctrl bit 3: Shift (right) bit 4: Shift (left) bit 5: Caps Lock OFF/ON bit 7,6 0,x: normal mode 1,0: GRPH mode 1,1: CODE mode Carry flag set =ASCII character Carry flag reset=CODE or GRAPH CHARACTER
REGISTERS PRESERVED	BC,DE,IX,IY AF',BC',DE',HL'
KILLBUF =	Kill key buffer
ENTRY:	0106H
ENTER:	Nothing
EXIT:	Nothing
REGISTERS PRESERVED	BC,DE,IX,IY AF',BC',DE',HL'

SETLOC =	Set Cursor Location
ENTRY:	0109H
ENTER:	H = X position (0 < = H < = 79) L = Y position (0 < = L < = 7)
EXIT:	Nothing.
REGISTERS PRESERVED	ALL
GETLOC =	Get Cursor Location
ENTRY:	010CH
ENTER:	Nothing.
EXIT:	H = X position L = Y position
REGISTERS PRESERVED	ALL except HL
SETCURSORONOFF =	Set Cursor on/off
ENTRY:	010FH
ENTER:	A =0: cursor blink on 1: cursor blink off (no cursor on screen)
EXIT:	Nothing.
REGISTERS PRESERVED	ALL except AF
SETCUTSORTYPE =	Set Cursor Type
ENTRY:	0112H
ENTER:	A =0: box cursor 1: underline cursor
EXIT:	Nothing.
REGISTERS PRESERVED	ALL except AF
SETCOLOR =	Set Character Color
ENTRY:	0115H
ENTER:	A =0: normal 1: reverse (highlight)
EXIT:	Nothing.
REGISTERS PRESERVED	ALL except AF
CHAROUT =	Output character to console ((DOES NOT SUPPORT ESC-sequence.))
ENTRY:	0118H
ENTER:	A = ASCII code to be output
EXIT:	Nothing.
REGISTERS PRESERVED	ALL
PUTCHAR =	Output character to console ((DOES SUPPORT ESC-sequence.))
ENTRY:	01A3H
ENTER:	A =ascii code to be output Supported commands are: 08H BS 09H TAB 0aH LF 0dH CR ESC A Cursor Up ESC B Cursor Down ESC C Cursor Right ESC D Cursor Left

	ESC H Cursor to Home ESC J Erase to end of screen ESC K Erase to end of line ESC Y Ln Clm Direct Cursor Address
EXIT:	Nothing
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
STROUT =	Output string to console ((DOES NOT SUPPORT ESC-sequence.))
ENTRY:	011BH
ENTER:	HL =string (must be null terminated.)
EXIT:	Nothing
REGISTERS PRESERVED	ALL except AF and HL
CLS =	Clear screen
ENTRY:	011EH
ENTER:	Nothing
EXIT:	Nothing
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
BEEP =	Beep a buzzer
ENTRY:	0121H
ENTER:	A = buzzer type (0:Low tone/1:High tone)
EXIT:	Nothing.
REGISTERS PRESERVED	ALL
CHECKCNCL =	Check that CNCL key is pushed NOW.
ENTRY:	0124H
ENTER:	Nothing
EXIT:	Carry Flag set =pushed. Carry Flag reset =not pushed.
REGISTERS PRESERVED	ALL except AF
PRNOUT =	Output one byte of data to printer
ENTRY:	0130H
ENTER:	A =data
EXIT:	Nothing.
REGISTERS PRESERVED	ALL except AF
PRNSTATUS =	Check printer status
ENTRY:	0133H
ENTER:	Nothing.
EXIT:	Zero Flag set =printer is ready. Zero Flag reset =printer is not ready.
REGISTERS PRESERVED	ALL except AF
READSLOT =	Read data in a slot
ENTRY:	0160H
ENTER:	A =slot number HL =offset (0 <= HL <= 0x3fff)
EXIT:	A =data
REGISTERS PRESERVED	ALL except AF

CHGSLOT =	Change slots.
ENTRY:	166H
ENTER:	A =slot number
EXIT:	Nothing.
REGISTERS PRESERVED	E,HL,IX,IY AF',BC',DE',HL'
CALLFAR =	Call routine in another slot. How to call: rst 30h db n ; slot number dw nn ; address
RSINIT =	Initial RS232C (Baud rate etc...)
ENTRY:	0140H
ENTER:	HL =Baud Rate etc .. H=0: 75 BPS =1: 110 BPS =2: 150 BPS =3: 300 BPS =4: 600 BPS =5: 1200 BPS =6: 2400 BPS =7: 4800 BPS =8: 9600 BPS =9: 19200 BPS L (BIT 7,6): STOP BIT 0,0: 0 0,1: 1 1,0: 1.5 1,1: 2 (BIT 5,4): PARITY CHECK x,0: Parity check disable 0,1: odd 1,1: even (BIT 3,2): DATA LENGTH 0,0: 5 bit 0,1: 6 bit 1,0: 7 bit 1,1: 8 bit (BIT 1): XON/XOFF handler execute bit 0: no execute 1: execute (BIT 0): timer interruption 0: enable 1: disable
EXIT:	Nothing.
REGISTERS PRESERVED	ALL
GETDATALEN =	Get the length of effective data in aux-buffer.
ENTRY:	0143H
ENTER:	Nothing.
EXIT:	HL =data length
REGISTERS PRESERVED	ALL except AF and HL

SENDDATA =	Output one byte of data to RS232C
ENTRY:	0146H
ENTER:	A =data
EXIT:	Carry Flag set: can't transfer. Carry Flag reset: no error
REGISTERS PRESERVED	ALL
GETDATA =	Get data from the aux-buffer.
ENTRY:	0149H
ENTER:	Nothing.
EXIT:	Zero Flag set =no data in aux-buffer Zero Flag reset =data exists. A =data E =status bit 7: FE (Framing Error) bit 6: OE (Overrun Error) bit 5: PE (Parity check Error)
REGISTERS PRESERVED	BC,HL,IX,IY AF',BC',DE',HL'
RSCLOSE =	Close RS232C
ENTRY:	014CH
ENTER:	Nothing.
EXIT:	Nothing.
REGISTERS PRESERVED	AF,DE,IX,IY AF',BC',DE',HL'
TAPEIN =	Read data from Tape
ENTRY:	0150H
ENTER:	Nothing.
EXIT:	Carry Flag set =Cancel key is pushed. Carry Flag reset=Ok A =data
REGISTERS PRESERVED	DE,HL,IX,IY AF',BC',DE',HL'
TAPEOUT =	Write data to Tape
ENTRY:	0153H
ENTER:	A =data
EXIT:	Carry Flag set =Cancel key is pushed. Carry Flag reset=Ok
REGISTERS PRESERVED	DE,HL,IX,IY AF',BC',DE',HL'
MOTORON =	Motor on
ENTRY:	0156H
ENTER:	Nothing.
EXIT:	Nothing.
REGISTERS PRESERVED	DE,HL,IX,IY AF',BC',DE',HL'
MOTOROFF =	Motor off
ENTRY:	0159H
ENTER:	Nothing.
EXIT:	Nothing.
REGISTERS PRESERVED	DE,HL,IX,IY AF',BC',DE',HL'

SYNCREAD =	Read Sync
ENTRY:	0169H
ENTER:	Nothing.
EXIT:	Carry Flag set =Cancel key is pushed. Carry Flag reset=Ok
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
SYNCWRITE =	Write Sync
ENTRY:	016CH
ENTER:	Nothing
EXIT:	Carry Flag set =Cancel key is pushed. Carry Flag reset=Ok
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
LINEIN =	Cooked line input
ENTRY:	01A6H
ENTER:	BC =length (BC < 80) DE =input location
EXIT:	A =last input character HL =string buffer (AP must copy this string to its buffer.)
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
LINEIN2 =	Cooked line input with default string
ENTRY:	01ACH
ENTER:	BC =length (BC < 80) DE =input location HL =default string (null terminated)
EXIT:	A =last input character HL =string buffer (AP must copy this string to its buffer.)
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
UNGETFORLINP =	Unget Char for LINEIN and LINEIN2
ENTRY:	01A9H
ENTER:	A = Character Code for unget
EXIT:	Nothing
REGISTERS PRESERVED	ALL
CMPHLDE =	Compare HL to DE

ENTRY:	20H
	How to call:
	LD HL,XXXX
	LD DE,YYYY
	rst 20H

ENTER:	HL/DE: data
EXIT:	Zero Flag set : HL==DE Zero Flag reset : HL!=DE Carry Flag set : HL < DE Carry Flag reset : HL <= DE
REGISTERS PRESERVED	ALL except Flag

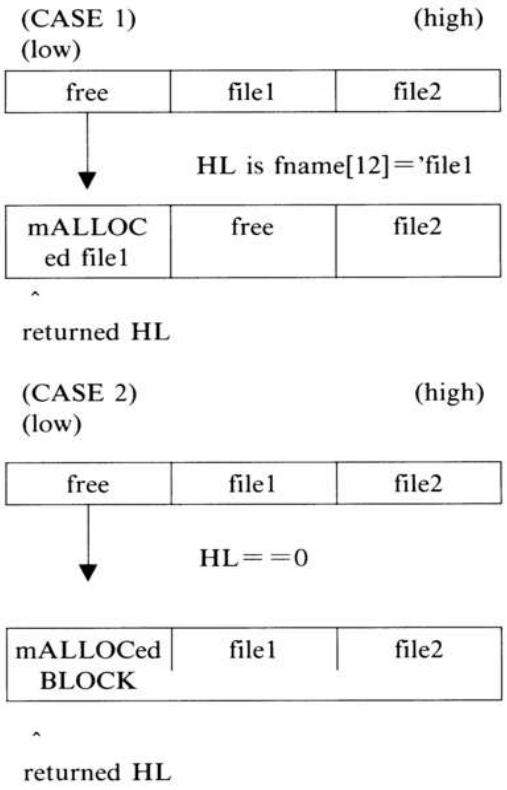
MALLOC =	Memory allocation
ENTRY:	0170H
ENTER:	HL =char fname[12]
EXIT:	Carry Flag set =error
	Carry Flag reset =no error
	HL =pointer to returned block
	DE =length of the block (32 bytes)

You can get a memory block by using this function.
When HL equals 0 , you can get all free blocks in RAM.

NOTE: This fname is not a string but a block. It is not null (0) terminated. An example of fname is:

```
;           123456789012
db          'foo     .bar'
```

Following is an example of the internal state:



REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
MCHGSIZE =	Changes the size of mALLOCed BLOCK.
ENTRY:	0173H
ENTER:	HL =length that you want (32-byte unit)
EXIT:	Carry Flag set =error
	Carry Flag reset =no error
	HL =new length of the block (32 bytes)
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'

MFREE =	Free mALLOCed BLOCK
ENTRY:	0176H
ENTER:	Nothing.
EXIT:	Carry Flag set =error Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
MCLOSE =	Close (save) mALLOCed BLOCK
ENTRY:	017CH
ENTER:	Nothing.
EXIT:	Carry Flag set =error Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
MNAME =	Names the mALLOCed BLOCK.
ENTRY:	017FH
ENTER:	HL =char fname[12]
EXIT:	Carry Flag set =error Carry Flag reset =no error NOTE: You must mName before mClosing. Otherwise you cannot ever open that block again.

An example of saving data to memory is:

1) Getting block (HL=0: get all free blocks)
2) Writing data in the block
3) Changing the size of the block
4) Naming
5) Closing the block

An example of editing the data in memory is:

1) Getting the block (HL: ptr to name)
2) Changing the size of the block to what you need
3) Editing the data
4) Closing the block

REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
LIST0 =	Initialize file listing AP must call this function before calling LIST-function.
ENTRY:	0182H
ENTER:	Nothing.
EXIT:	Nothing.
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
LIST =	Get file list This function returns the file list.
ENTRY:	0185H
ENTER:	DE =fcb pointer A =0: next file 0xff: previous file
EXIT:	Carry Flag set: no more files Carry Flag reset: no error

This is a sample:

```
        struct fcb {
                char        device;
                char        name[12];
                int         filelength;
                char        reserved[17];
        };
        /* sizeof(struct fcb) is 32 */
        /* device */
        #define DevMemory      0x01
        #define DevICram       0x02
        #define DevDriveA      0x11

void main( ) {
        void ls( );
        ls(DevMemory);
        ls(DevICram);
        ls(DevDriveA);

{
ls(device)char device;
        int i;
        struct fcb myfcb;
        fcb.device=device;
        list0();
        for(;;)
                if( -list((char)0,fcb) )break;
                        /* A:=0 , DE:=fcb */
                for(i=0;i<12;++i)putchar(fcb.name[i]);
                putchar('¥n');

        }
/* where
        -list: call list
               sbc  a,a ; sub with carry
               ret
*/
}
```

REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
OPEN =	Open a file This function opens a file and sets up an fcb.
ENTRY:	0188H
ENTER:	DE =fcb pointer A =0: make a new file in write mode 1: open a file in append-write mode 2: open a file in read mode
EXIT:	Carry Flag set =error Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'

READ =	Read a file.
ENTRY:	018BH
ENTER:	DE =fcb pointer
	HL =buffer pointer (size is 128)
EXIT:	Carry Flag set =error
	Carry Flag reset =no error
	A =read byte.
REGISTERS PRESERVED	IX,IY
	AF',BC',DE',HL'
WRITE =	Write a file
ENTRY:	018EH
ENTER:	DE =fcb pointer
	HL =buffer pointer
EXIT:	Carry Flag set =error
	Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY
	AF',BC',DE',HL'
CLOSE =	Close a file
ENTRY:	0191H
ENTER:	HL =fcb pointer
EXIT:	Carry Flag set =error
	Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY
	AF',BC',DE',HL'
DELETE =	Delete a file
ENTRY:	0194H
ENTER:	HL =fcb pointer
EXIT:	Carry Flag set =error
	Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY
	AF',BC',DE',HL'
RENAME =	Rename a file.
ENTRY:	0197H
ENTER:	HL =NewNameFcb pointer
	DE =OldNameFcb pointer
EXIT:	Carry Flag set =error
	Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY
	AF',BC',DE',HL'
FORMAT =	Format a disk-device.
ENTRY:	019AH
ENTER:	A = device number
	02H: internal RAM disk
	03H: IC RAM card
	11H: disk drive
EXIT:	Carry Flag set =error
	Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY
	AF',BC',DE',HL'

DEVROOM =	Get device's rest size.
ENTRY:	01C1H
ENTER:	A = device number 02H: internal RAM disk 03H: IC RAM card 11H: disk drive
EXIT:	Carry Flag set =error Carry Flag reset =no error HL =room left in 128-byte unit
EXIT:	
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
SEEK =	SEEK FILE POINTER (only for RAM disk file and IC card RAM disk file)
ENTRY:	01BEH
ENTER:	HL =fcb pointer DE =seek pos from head
EXIT:	Carry Flag set =error Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
WAIT =	Wait for fix time.
ENTRY:	01A0H
ENTER:	A = time for wait in 1/100 sec unit
EXIT:	Nothing
REGISTERS PRESERVED	BC,DE,HL,IX,IY AF',BC',DE',HL'
RUNIC =	Run IC card program.
ENTRY:	01AFH
ENTER:	Nothing
EXIT:	Depends on card program.
REGISTERS PRESERVED	Depends on card program.
RUNFILE =	Run a program file.
ENTRY:	01B2H
ENTER:	HL =fcb pointer File header is: db 'PR' ; id dw Size ; program size dw entry ; entry of program dw load ; load address. If 0, then normal.
EXIT:	Nothing.
REGISTERS PRESERVED	Depends on program
POFFCOUNTPOINTER =	Get Power off counter pointer.
ENTRY:	01B5H
ENTER:	Nothing.
EXIT:	HL =pointer to power off counter
REGISTERS PRESERVED	IX,IY AF',BC',DE',HL'
SETBTYPE =	Set battery type.
ENTRY:	01B8H
ENTER:	A =0 :Alkaline 1 :Ni-Cd
EXIT:	Nothing.
REGISTERS PRESERVED	HL,IX,IY AF',BC',DE',HL'

GETWORK =	Get Work Area
ENTRY:	01BBH
ENTER:	HL = address that AP wants to get
	if (HL=0) free work area
EXIT:	Carry Flag set =error
	Carry Flag reset =no error
REGISTERS PRESERVED	IX,IY
	AF',BC',DE',HL'

2. SPELLER INFORMATION

The speller/thesaurus code contains a single entry point at hex 2C00. This software hook is from 2C00H to 2C1FH. The function to be executed is contained in the A register. The speller/thesaurus code sets the correct program/data base bank and performs the desired function.

Note: No registers are preserved by the speller/thesaurus module. To be safe, assume all registers (of the current register bank) are destoyed by call.

User Dictionary
This dictionary is user-defined and implemented. The spelling corrector does not reference the user dictionary.

Operations
The A register contains the function code. The chart below details any other required data. All strings should be null (0) terminated.

Code	Input	Function	Outputs
1	A=2 (H, L) = string addr.	Spell String	C=1 if OK =0 if misspelled
2	A=3 (H, L) = string addr.	Single Char. Corrections	C=1 if alternates (H,L)=ptr to 1st Alt. A=# of alternates
3	A=4 (H, L) = string addr.	Phonetic Corrections	C=1 if alternates (H,L)=ptr to phonetic Alt. A=# of alternates
4	A=10	Find Synonyms	C=1 if more synonyms C=0 if only one synonym (H,L)=ptr to 1st syn. A=# of synonyms in this row B=0 (noun) 1 (verb) 2 (adjective) 3 (adverb) 4 (preposition) 7 (conjunction)
5	A=11	Next Syn. Row	C=0 if no more rows C=1 if more rows exist (H,L) =addr. of 1st syn. on a row B=0 (noun) 1 (verb) 2 (adjective) 3 (adverb) 4 (preposition) 7 (conjunction)
6	A=12	Previous Syn.	C=0 if at top C=1 if there's a row above (H,L) =addr. of syn. on a row A=# syns in this row B=0 (noun) 1 (verb) 2 (adjective) 3 (adverb) 4 (preposition) 7 (conjunction)

Note: Single Character Correction
This routine would take care of alternates allowing single character rules to get
(1) DELETED (2) TRANSPOSED (3) INSERTED (4) REPLACED.

The organization of the synonyms is as follows:

<Main Syn 1> <Next Main Syn 1> <alt syn 11> <alt syn 12> ... <alt syn 1N[1]>

<Main Syn 2> <Next Main Syn 2> <alt syn 21> <alt syn 22> ... <alt syn 2N[2]>

.

.

.

<Main Syn m> <Next Main Syn m> <alt syn m1> <alt syn m2> ... <alt syn mN[n]>

where N[1], N[2], ... N[n] are the lengths of row 1, row 2 and row n, respectively, and m is the number of rows. Note that each row can have a different number of synonyms. The first two synonyms on a row contain the most "popular" alternate meanings of the root word. The rest of the list contains more esoteric definitions.

A call to Find Synonyms returns in the A register the number of synonyms in the first row. The (H,L) points to the first string of the row. Each string is null terminated.

The locations for the counts and the quit alternate flags are as follows:

Single character correction (function 3) 8325H
Phonetic corrections (function 4) 8326H
Quit corrections 8327H

When the Corrections are in progress and the byte 0FFH is written to quit corrections (location 8327H), then the correction function 3 or 4 returns.

String Format

All strings are returned in the following format:

<string 1> <0> <string 2> <0> ... <string n> <0>

The A register contains the total number of strings that the (H,L) register pair points to.

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1A0

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